

[54] EDGE SMOOTHING FOR REAL-TIME SIMULATION OF A POLYGON FACE OBJECT SYSTEM AS VIEWED BY A MOVING OBSERVER

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[58] Field of Search 364/515, 555, 522, 521, 364/578; 358/166, 103, 104, 135, 160; 35/10.2, 10.24; 340/728, 723, 724

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Primary Examiner—Errol A. Krass

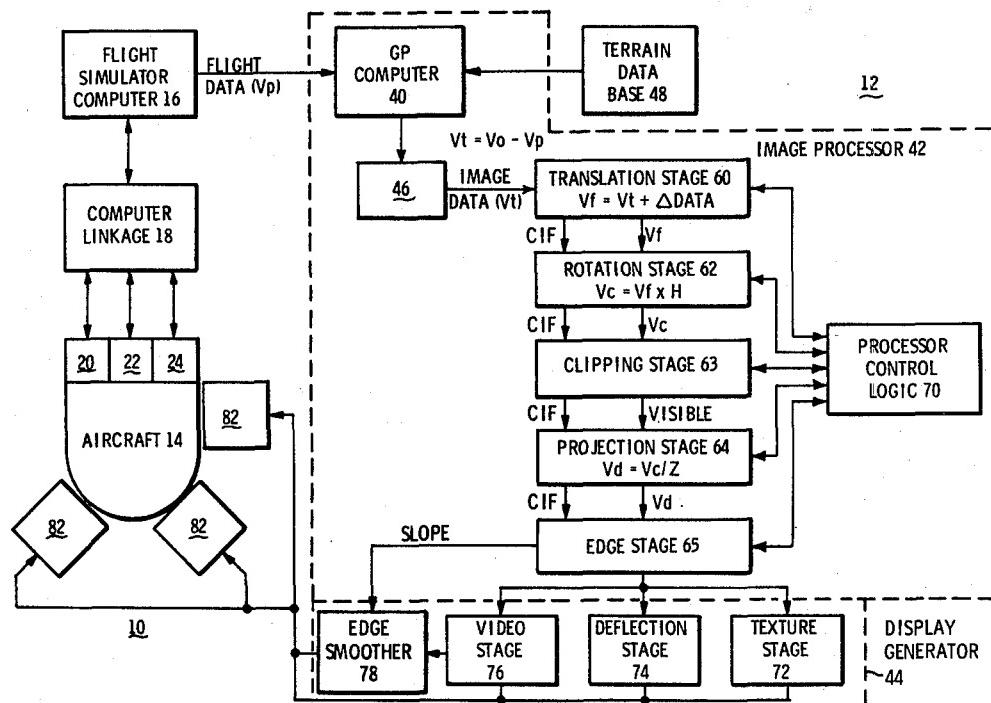
Attorney, Agent, or Firm—Paul Hentzel; Jeff Rothenberg

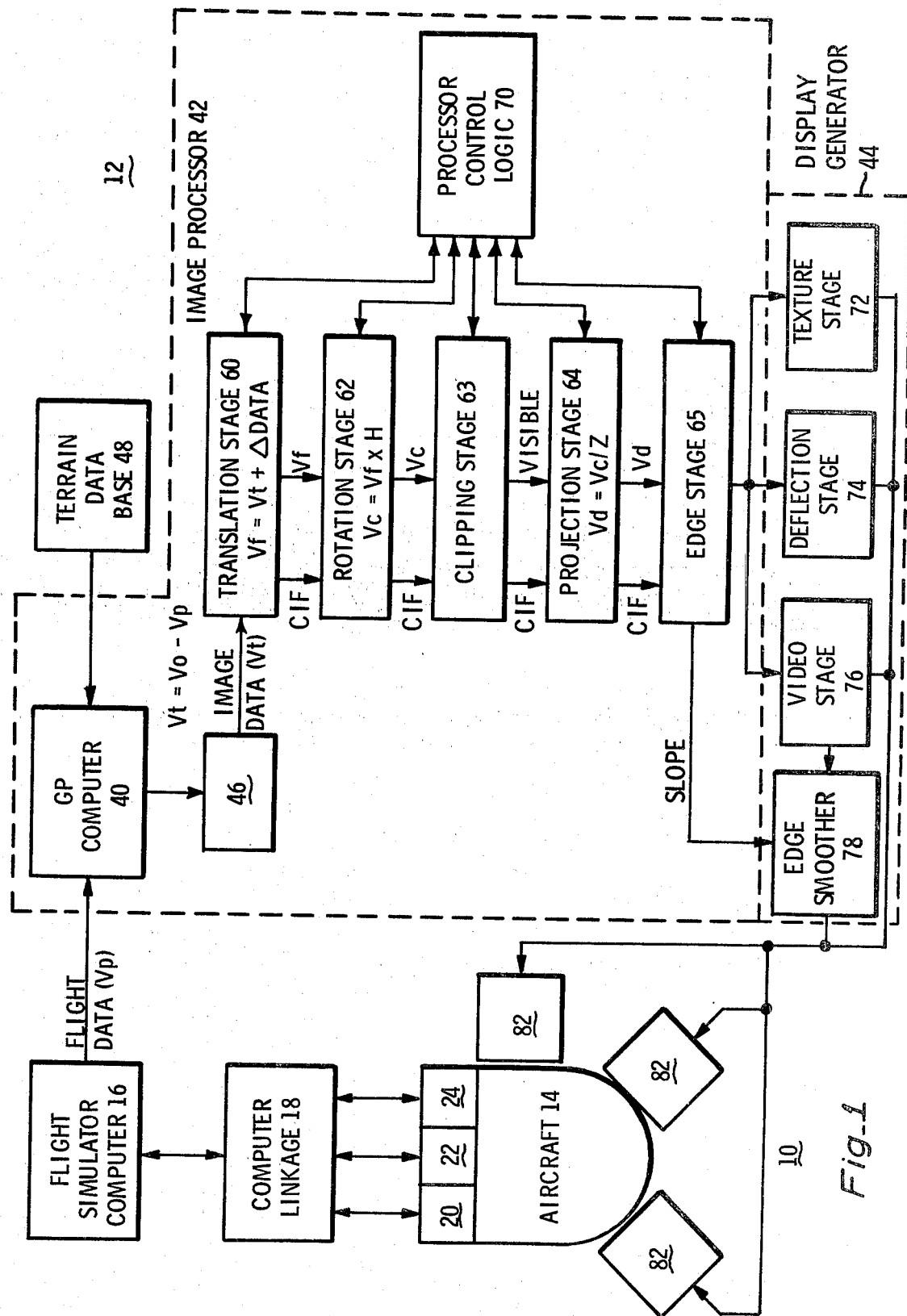
[57] ABSTRACT

The visual system within an aircraft flight simulation

system receives flight data and terrain data which is formatted into a buffer memory. The image data is forwarded to an image processor which translates the image data into face vertex vectors V_f , defining the position relationship between the vertices of each terrain object and the aircraft. The image processor then rotates, clips, and projects the image data into two-dimensional display vectors (V_d). A display generator receives the V_d faces, and other image data to provide analog inputs to CRT devices which provide the window displays for the simulated aircraft. The video signal to the CRT devices passes through an edge smoothing device which prolongs the rise time (and fall time) of the video data inversely as the slope of the edge being smoothed. An operational amplifier within the edge smoothing device has a plurality of independently selectable feedback capacitors each having a different value. The values of the capacitors form a series which doubles as a power of two. Each feedback capacitor has a fast switch responsive to the corresponding bit of a digital binary control word for selecting (1) or not selecting (0) that capacitor. The control word is determined by the slope of each edge. The resulting actual feedback capacitance for each edge is the sum of all the selected capacitors and is directly proportional to the value of the binary control word. The output rise time (or fall time) is a function of the feedback capacitance, and is controlled by the slope through the binary control word.

25 Claims, 17 Drawing Figures





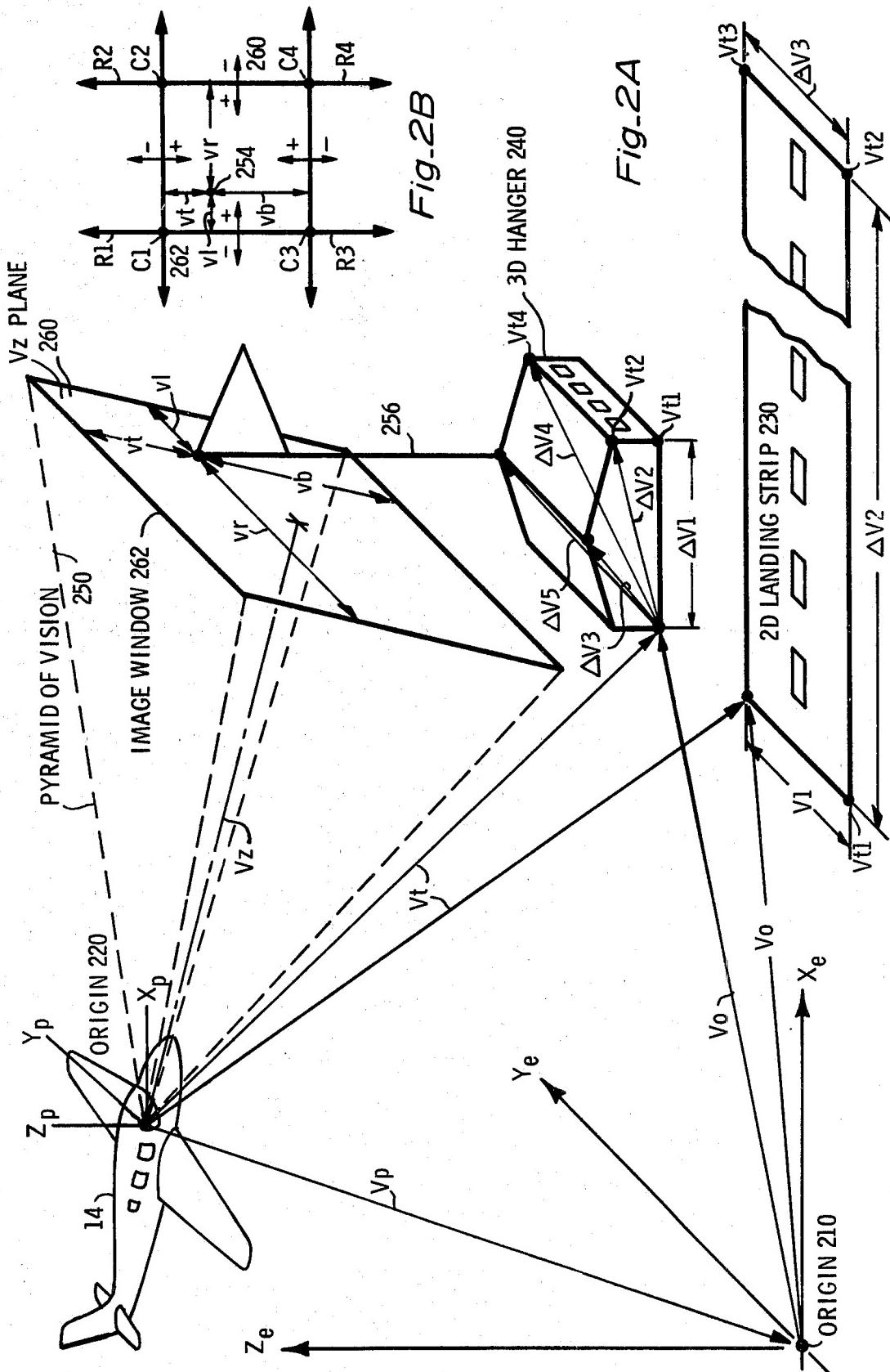
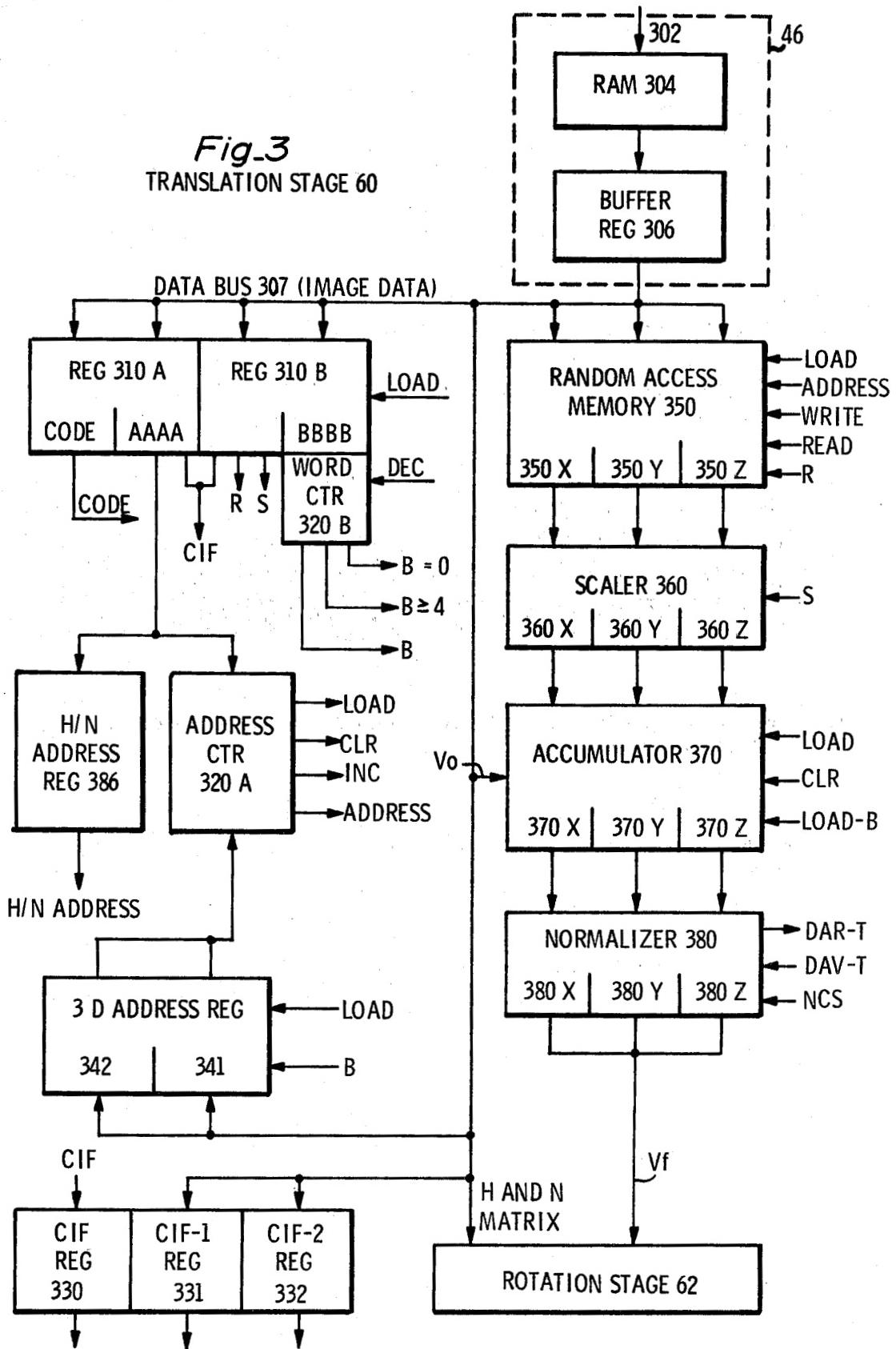


Fig. 3
TRANSLATION STAGE 60



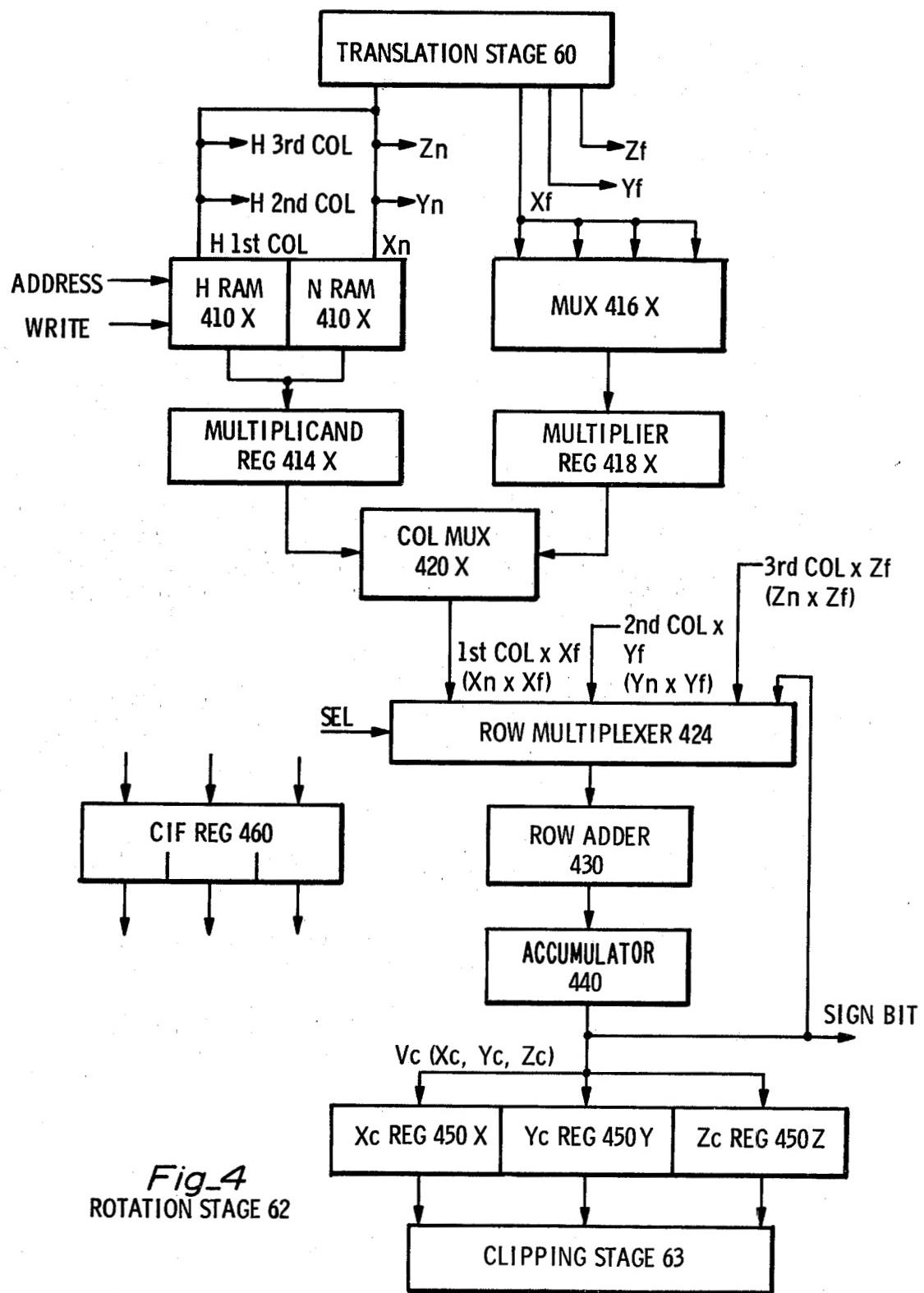
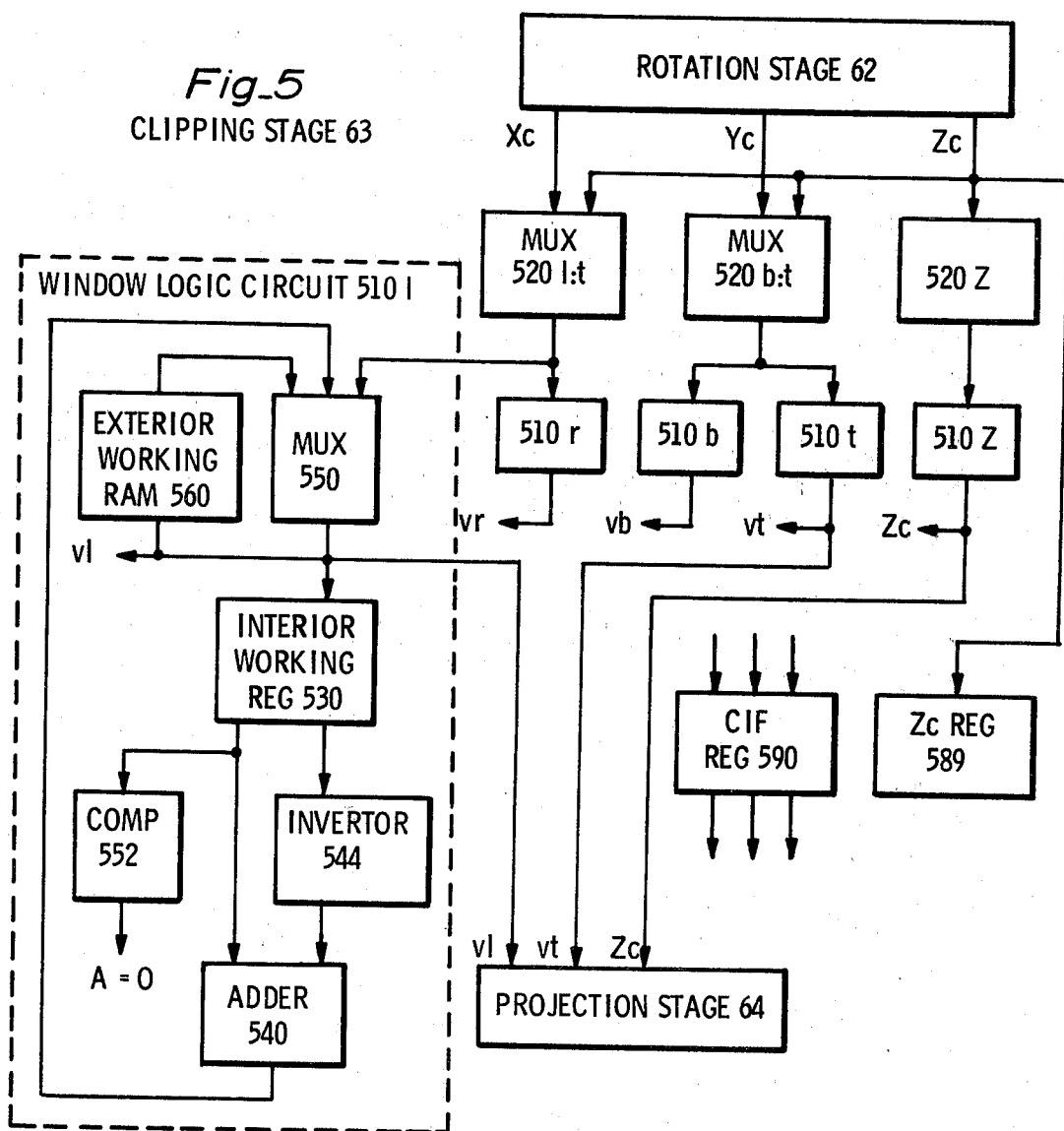
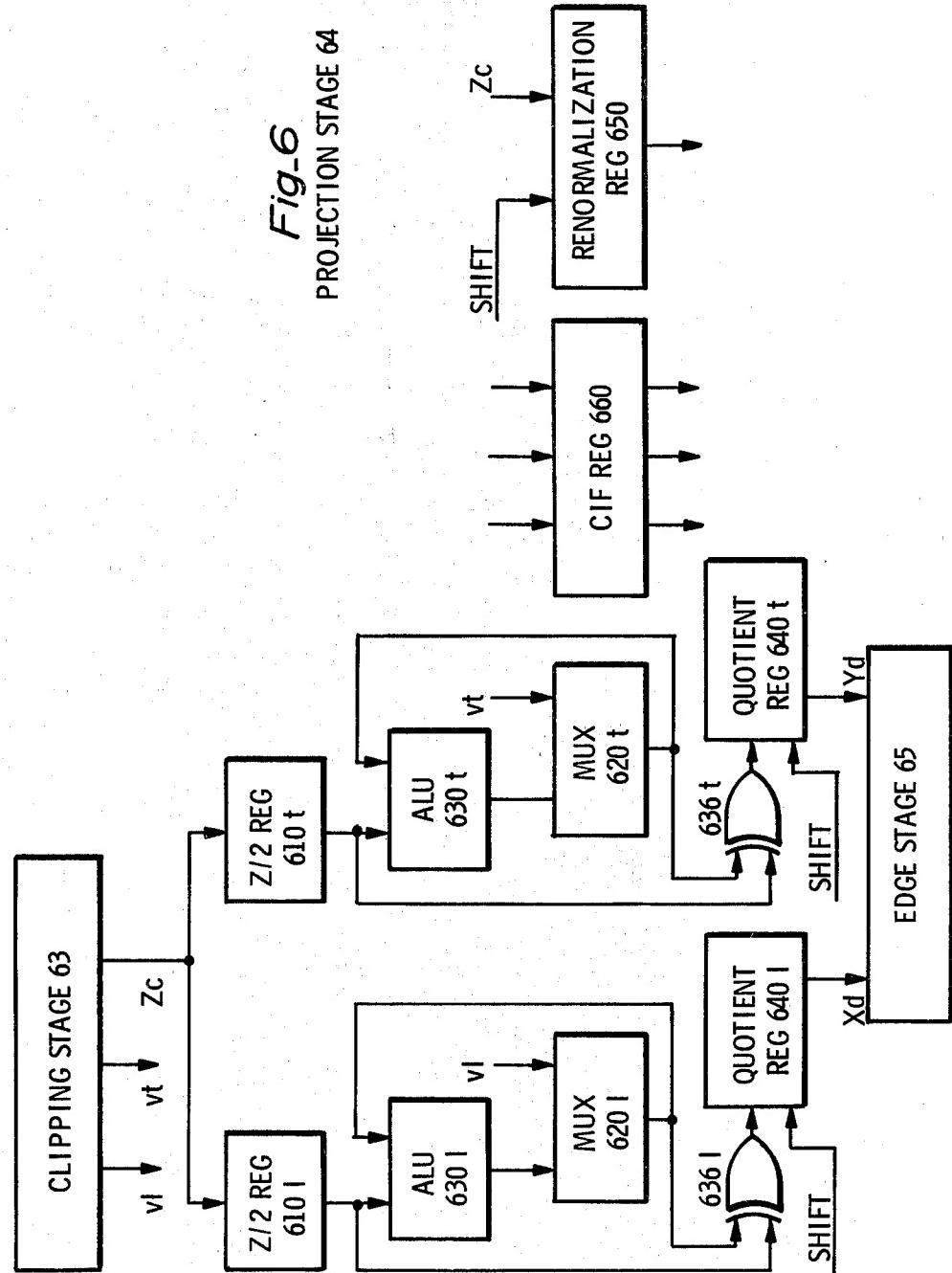


Fig. 4
ROTATION STAGE 62





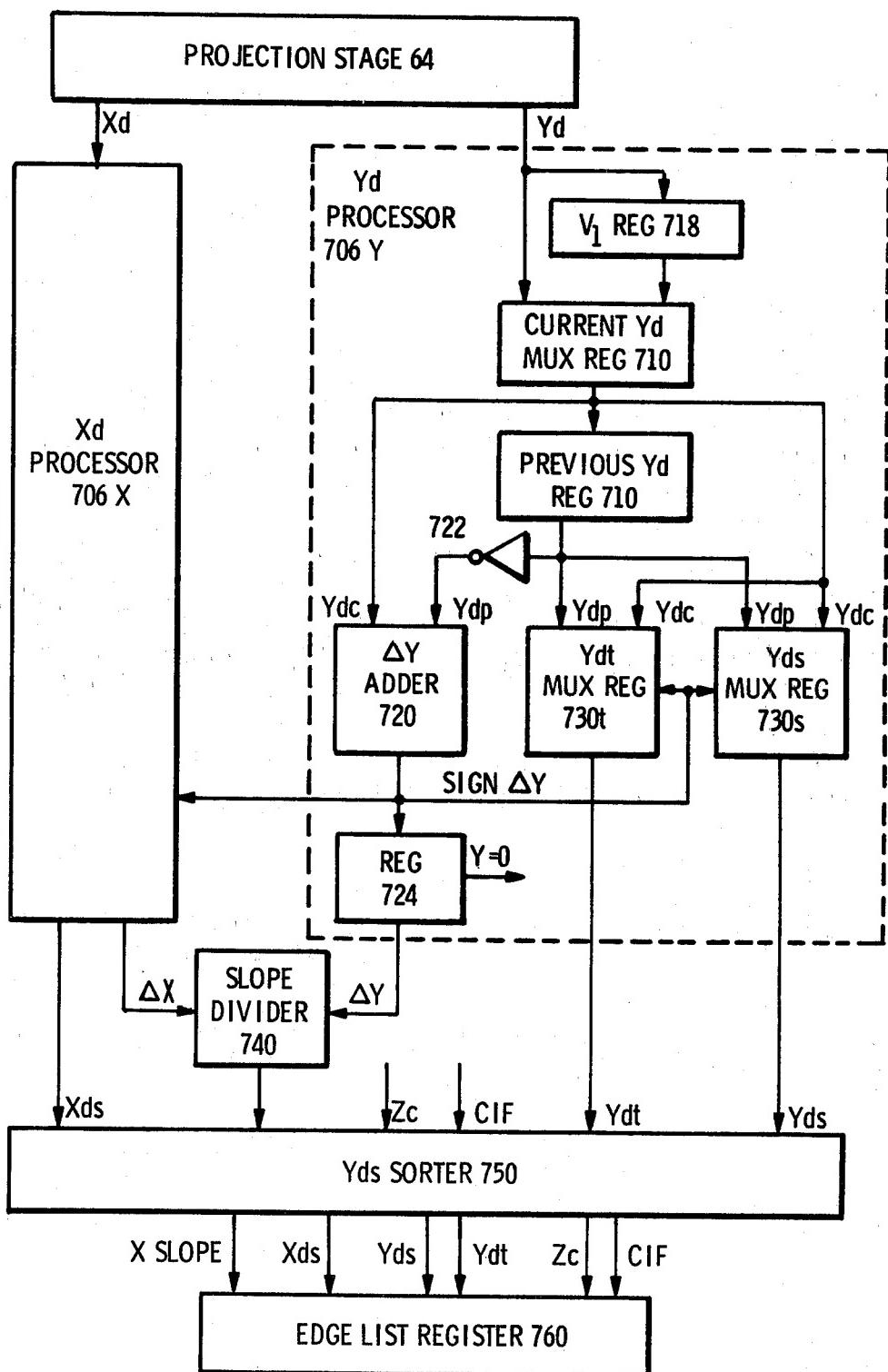


Fig. 7
EDGE STAGE 65

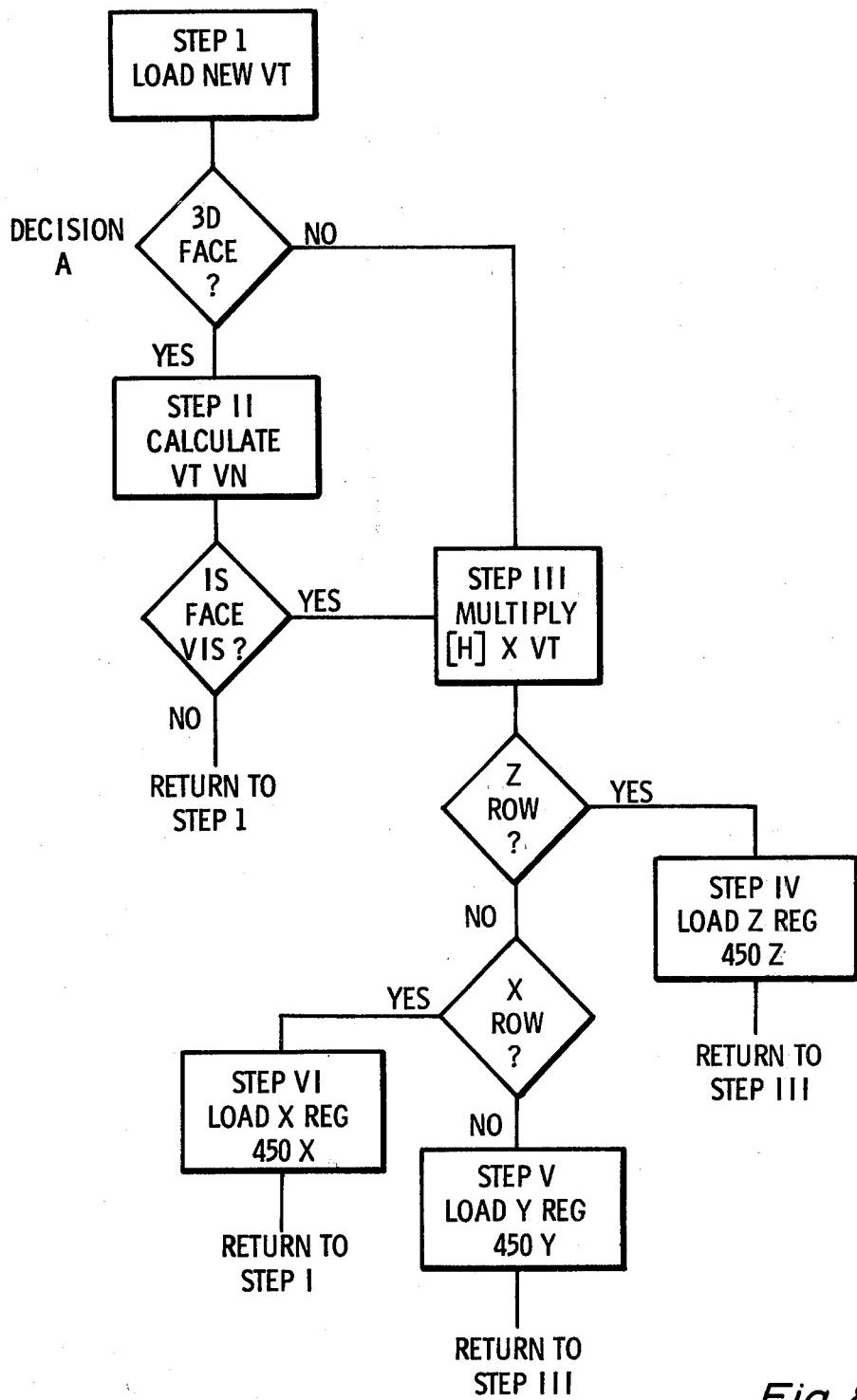


Fig.-8A
ROTATION CONTROL

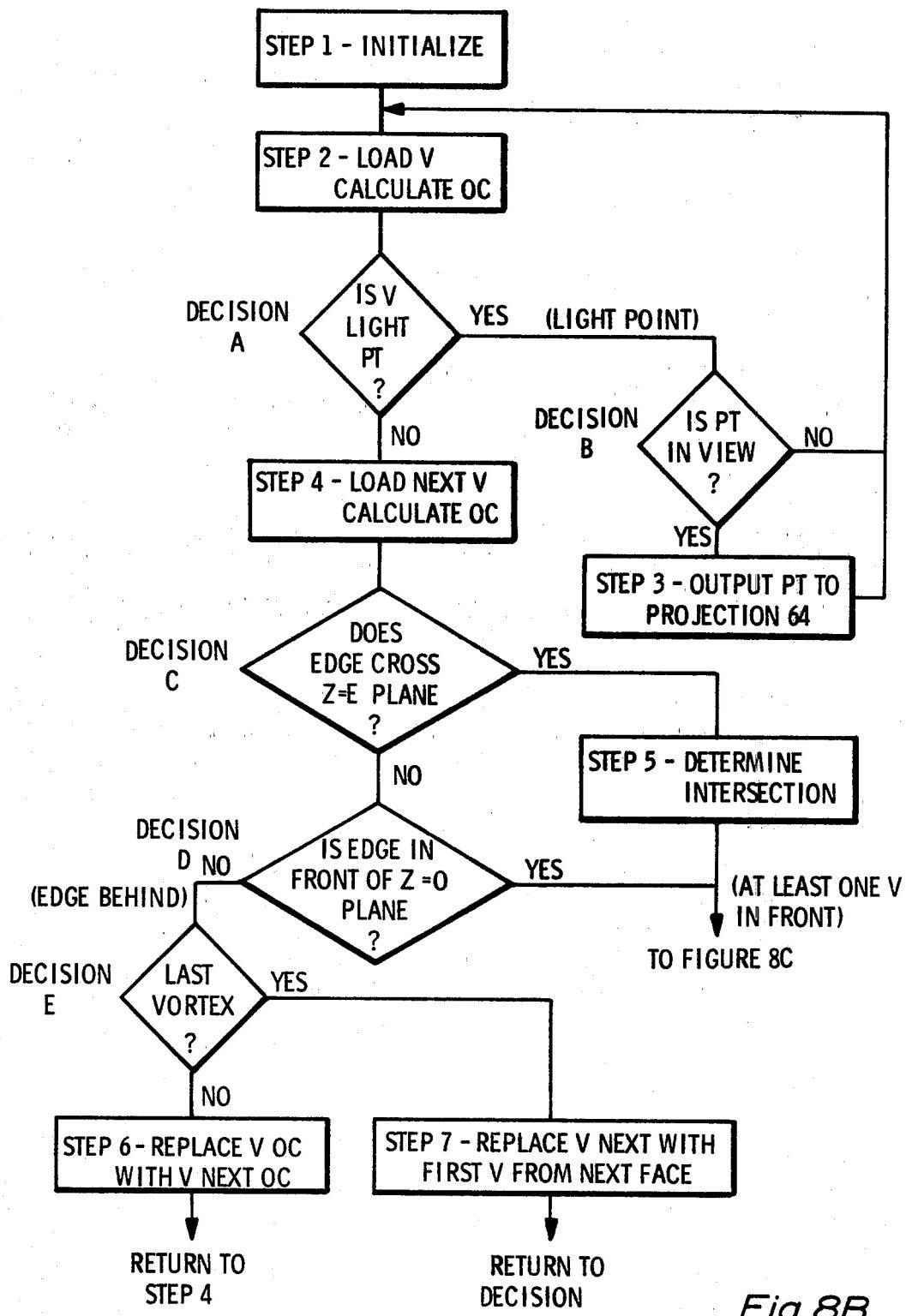
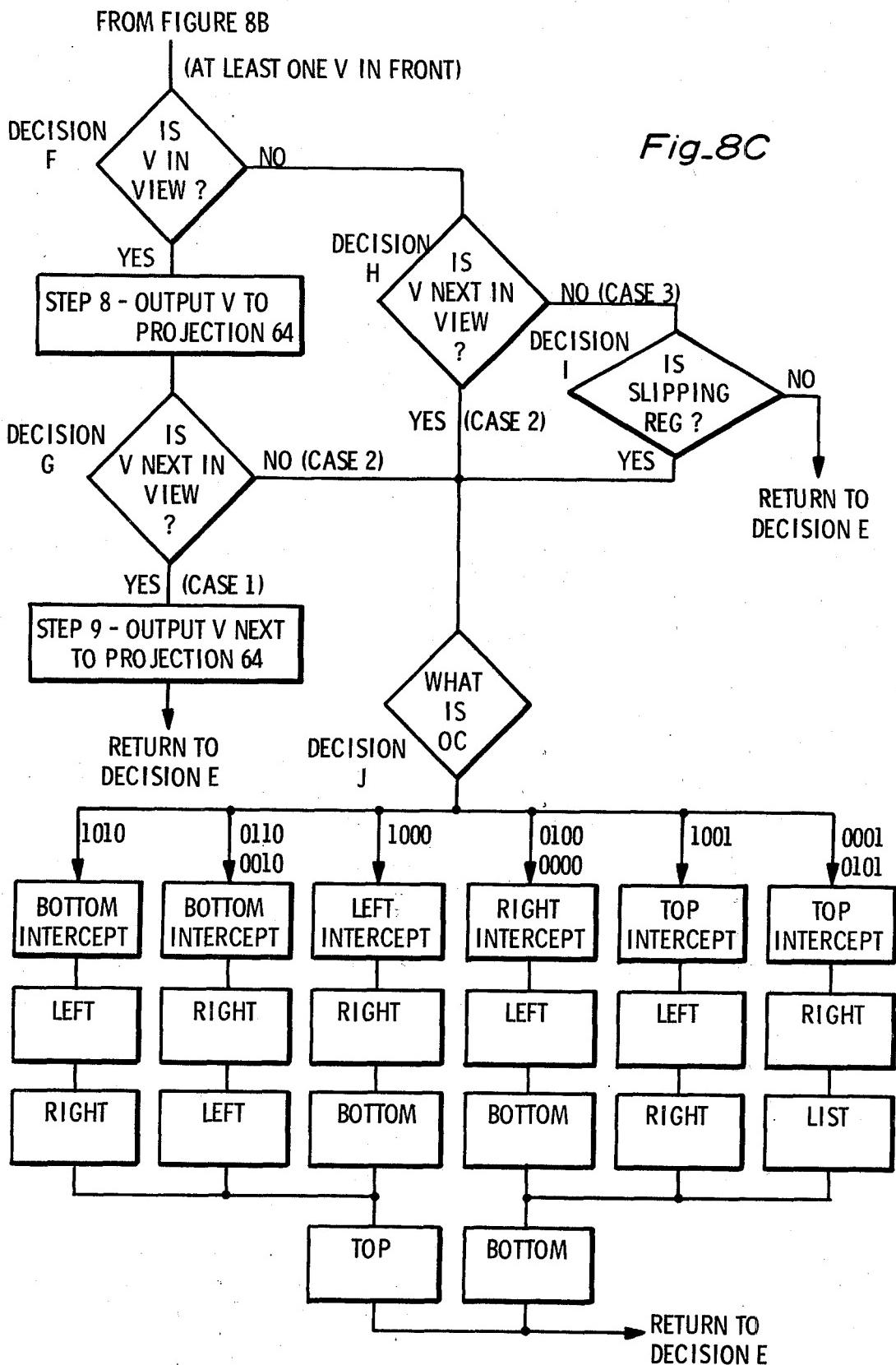
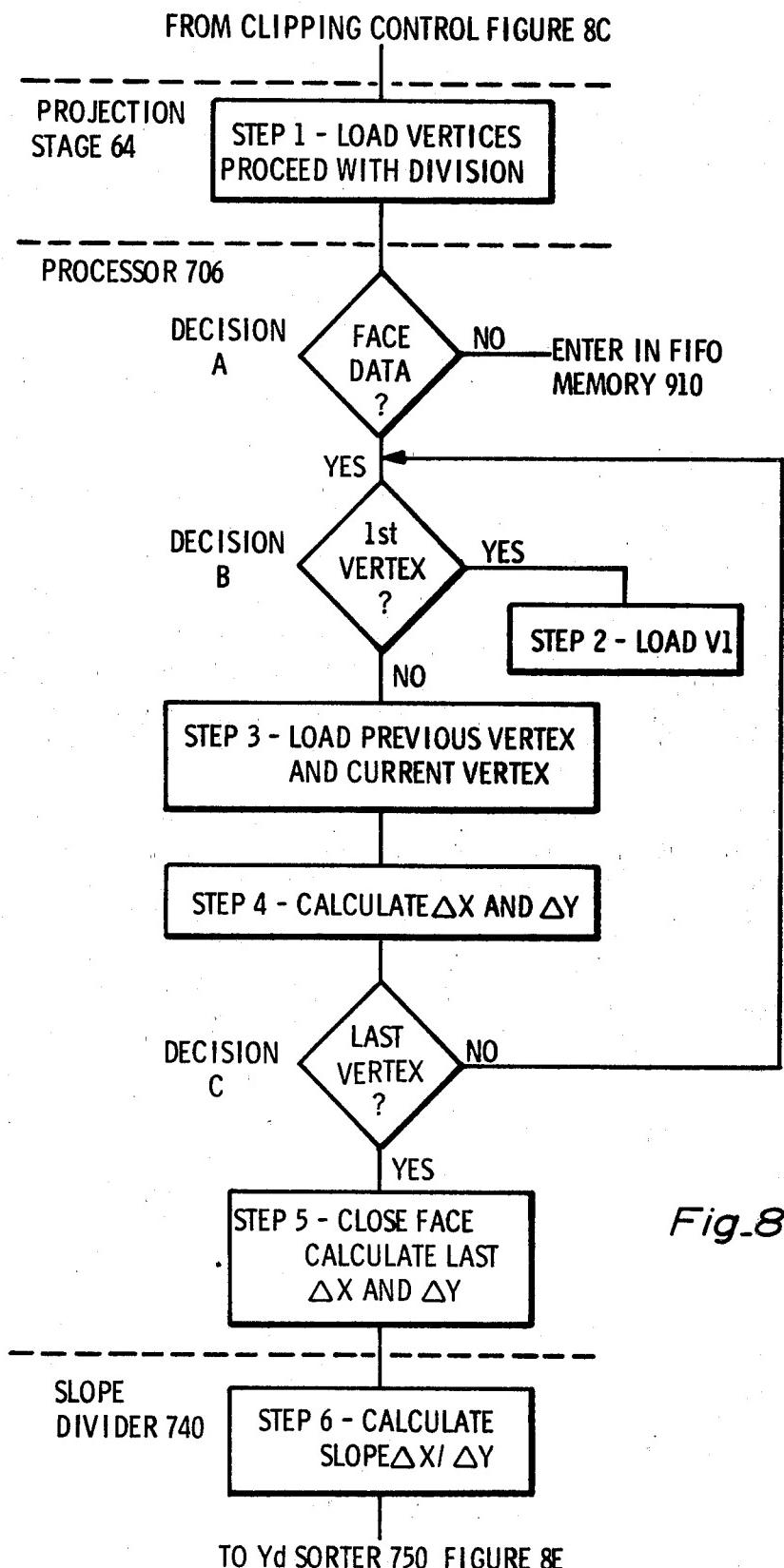
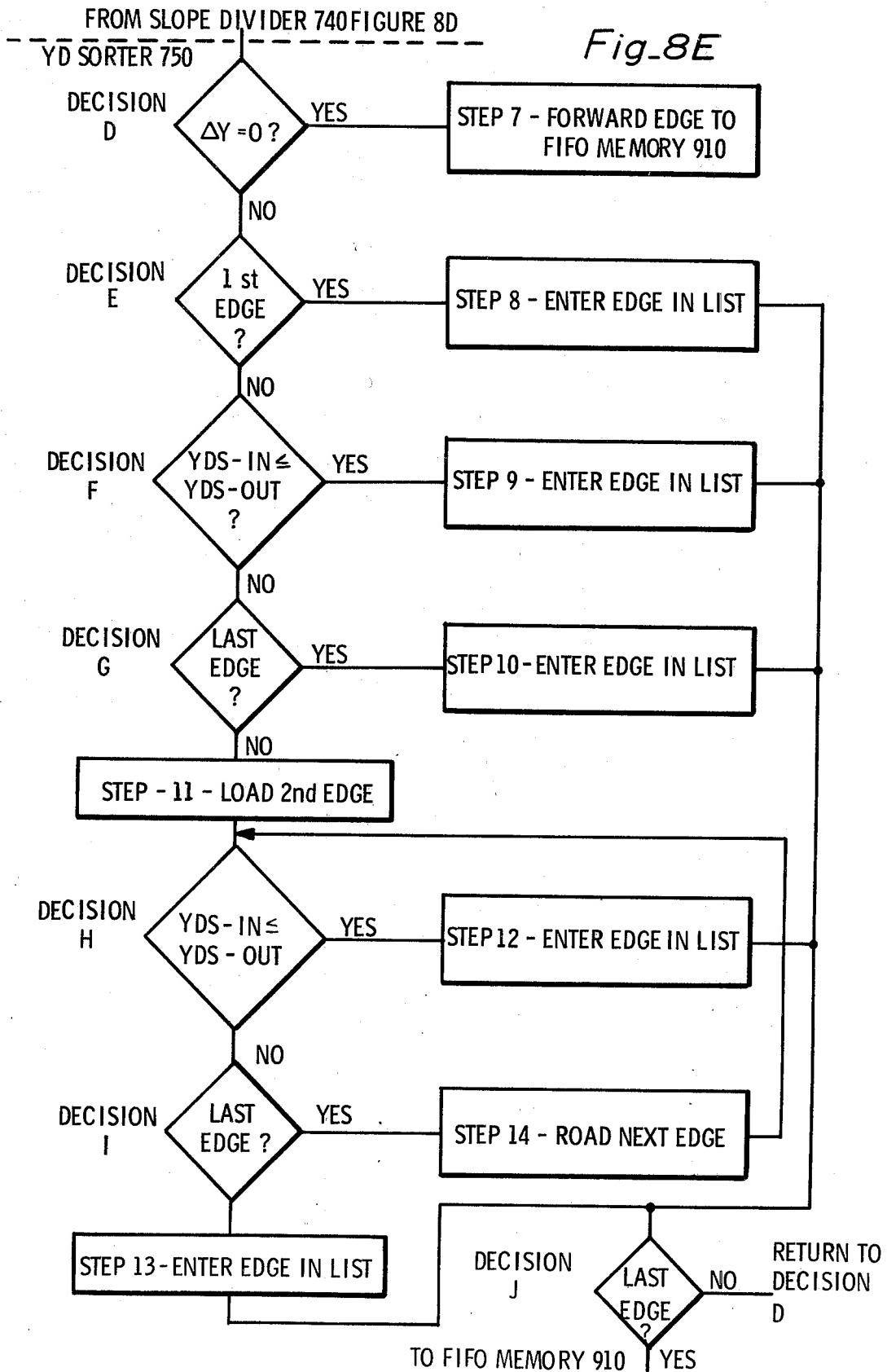
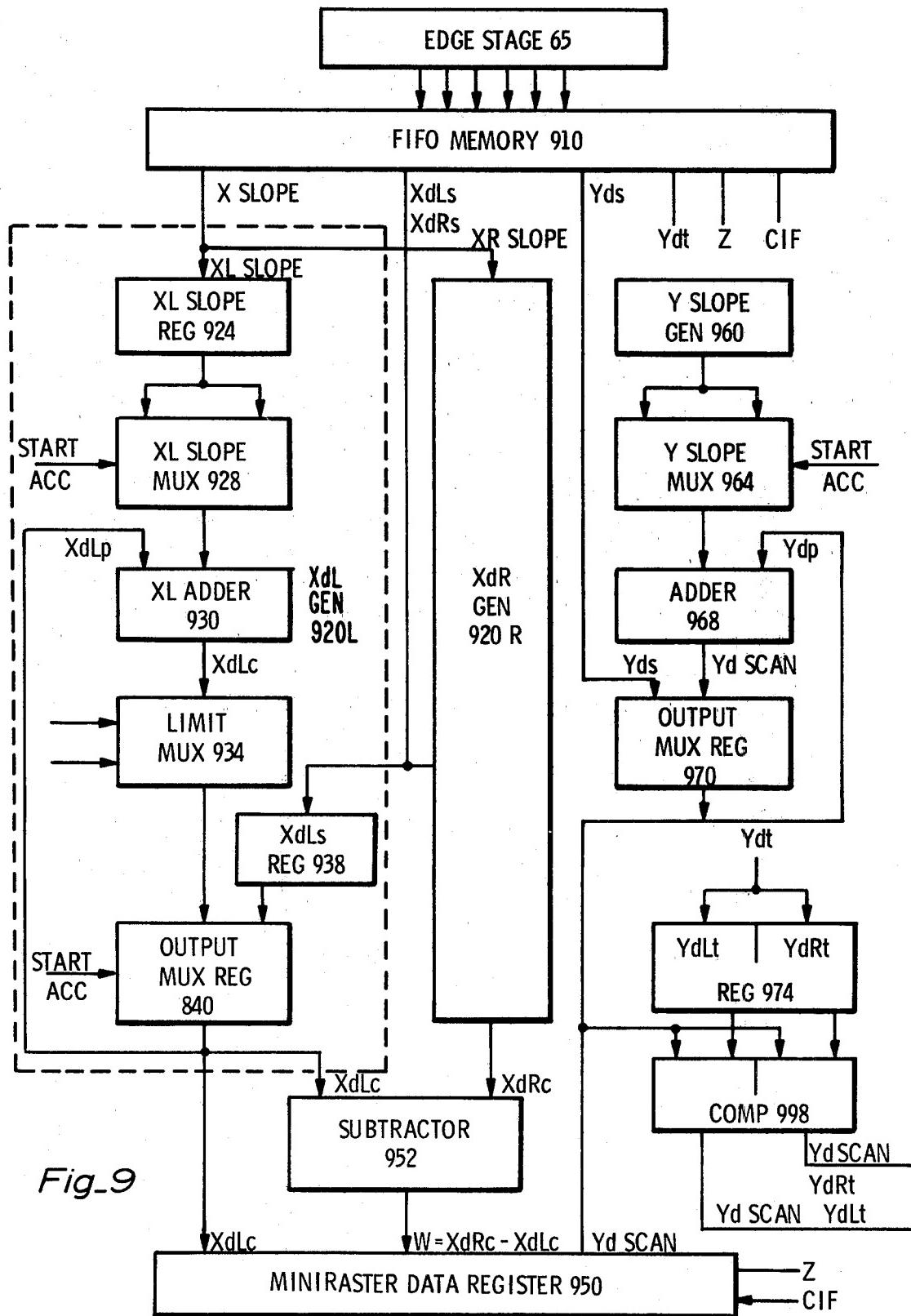


Fig. 8B
CLIPPING CONTROL









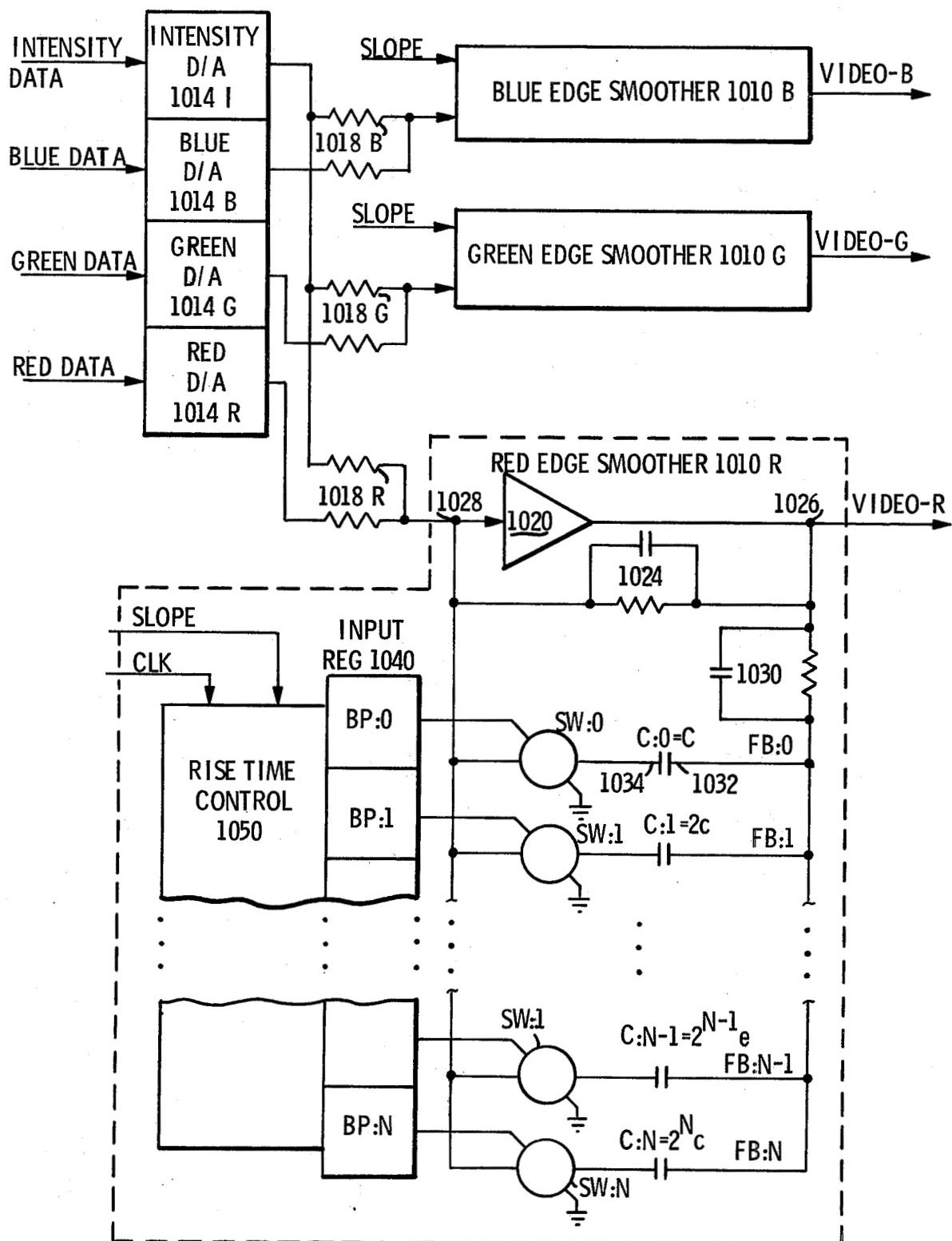


Fig. 10

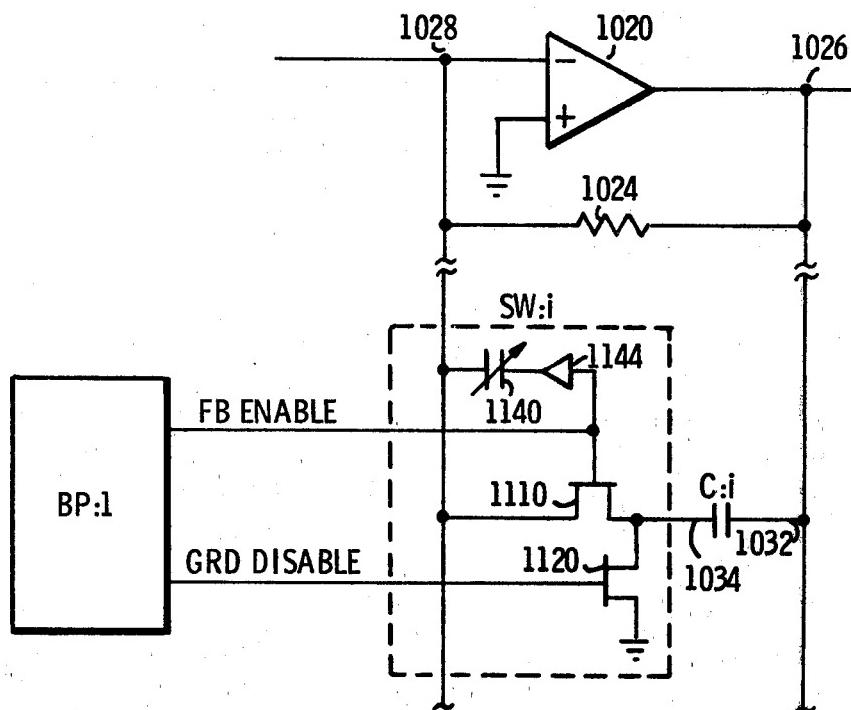


Fig-11

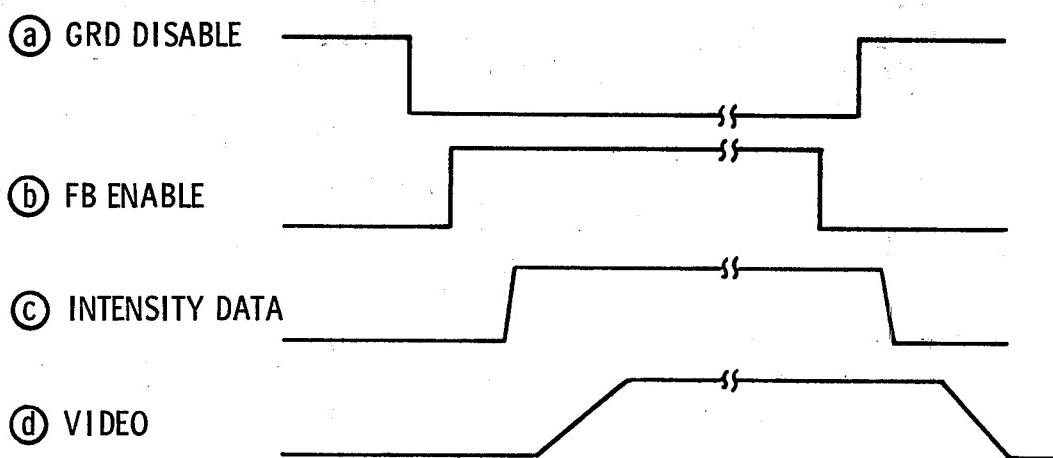


Fig-12

**EDGE SMOOTHING FOR REAL-TIME
SIMULATION OF A POLYGON FACE OBJECT
SYSTEM AS VIEWED BY A MOVING OBSERVER**

The invention described herein was made in the performance of work under NASA Contract Number NAS9-14910 and is subject to the provisions of Section 305 of the National Aeronautics and Space Act of 1958 (72 Stat. 435; 42 U.S.C. 2457).

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BACKGROUND OF THE INVENTION

This invention relates to edge smoothing of digitally generated images and more particularly employing a variable rise time to blend adjacent intensities.

Heretofore, digital image generated (DIG) displays exhibited a "staircase" effect along face edges caused by the discrete changes in video intensity at specific X locations inherent in digital data. Horizontal edges (slope=0) were unaffected by this digital characteristic because they involved a single scanline (delta Y=0) with a single step at the start of the edge. As the horizontal edge was tilted upward or downward (delta Y \neq 0) steps appear, one step for each horizontal scanline encompassed by the delta Y for that edge. As the edge approached a vertical position (slope approaches infinity) the steps increase in number but also become much smaller in amplitude (delta X approaches 0) and hence less visible. Previous techniques to smooth sloping edges involved massaging the digital data to provide a series of smaller step changes in intensity instead of a single step change. The resulting family of adjacent stair steps were less visible than the unsmoothed single staircase.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide an improved, low-cost edge smoothing device which requires a minimum of circuitry.

It is another object of this invention to provide an analog edge smoothing device.

It is a further object of this invention to provide an edge smoothing device which controls the rise time for the video signal.

It is yet another object of this invention to provide an edge smoother which is responsive to the slope of the edge being smoothed.

It is yet a further object of this invention to provide a noise-free edge smoothing device.

It is still another object of this invention to provide an edge smoothing device which is simple to implement into an imaging system.

It is still a further object of this invention to provide a circuit which edge smooths intensity and color.

It is another object of this invention to provide an edge smoothing circuit having a rise time RC constant generally equal to the pitch of steps along the scanline.

DESCRIPTION OF THE FIGURES

- 15 Further objects and advantages of the present invention, and the operation of the visual system, will become apparent from the following detailed description taken in conjunction with the drawings, in which:
 - FIG. 1 is a block diagram of DIG visual system 10 and peripheral flight simulation equipment showing data flow relationships;
 - FIG. 2a is a pictorial representation of an aircraft and several terrain features illustrating the image vectors;
 - 25 FIG. 2b is a block diagram showing outcoding regions;
 - FIG. 3 is a block diagram of translational stage 60 wherein the delta data is translated into face vertex vectors Vf;
 - 30 FIG. 4 is a block diagram of rotation stage 62 wherein each Vf is multiplied by an H matrix;
 - FIG. 5 is a block diagram of clipping stage 63 which eliminates image data outside the field of vision;
 - 35 FIG. 6 is a block diagram of projection stage 64 wherein Xc and Yc are divided by Zc to project Vc into the X-Y plane;
 - FIG. 7 is a block diagram of edge stage 65 which identifies the edge of each polygon face and the slopes thereof;
 - 40 FIGS. 8A-E is a logic diagram of the processor control logic 70;
 - FIG. 9 is a block diagram of the miniraster calculator 72 which provides the miniraster for each polygon face;
 - FIG. 10 is a general schematic diagram of the edge smoothing device;
 - 45 FIG. 11 is a detailed schematic of the ith feedback of the edge smoothing device; and
 - FIG. 12 is a timing diagram for the switching of the edge smoothing device.

GENERAL DESCRIPTION OF FLIGHT SIMULATION SYSTEM 10

- 50 FIG. 1 shows a flight simulation system 10 with visual capabilities provided by a digital visual system 12. A simulated aircraft 14 is linked to flight simulation computer 16 and visual system 12 through computer linkage 18. Flight computer 16 controls motion system 20 and instrument system 22 of aircraft 14 in response to the pilot's maneuvering action at aircraft controls 24.
- 55 Visual system 12 is formed by general purpose computer 40 (such as Digital Equipment Corporation PDP 11/35) plus image processor 42, display generator 44, and interface controller 46. Interface controller 46 is provided to process flight data from aircraft 14 to image processor 42 and to control image data flow from GP computer 40 to image processor 42 via a data buffer.
- 60 GP computer 40 receives flight data, such as aircraft position Vp, aircraft roll, pitch, and yaw attitude (H

matrix), etc. from computer 16. GP computer 40 additionally receives terrain data (both natural formations and cultural structures) from data base 48 such as runways, towers, hangers, roads, rivers, fields, moving objects, etc. In general visual system 12 may process and display terrain features consisting of points, lines, closed convex polygons, or combinations thereof. Preferably the aircraft position data is an aircraft position vector V_p extending from the simulated position of aircraft 14 to the origin of the terrain coordinate system (see FIG. 2). In order to simplify conception and data organization, the terrain origin is preferably located proximate the touchdown area of the runway, and the x axis of the terrain coordinate system from data base 48 is coincident to the runway centerline. An updated V_p is supplied each frame period by flight simulation computer 16 as the flight parameters of aircraft 14 change. The earth data also includes the position of certain landmark points (V_o) such as the first vertex of each face, and the relative position of the points forming other terrain features (delta data). Translation stage 60 subtracts V_p from each V_o to form translated vectors ($V_t = V_o - V_p$). Translation stage 60 then combines the delta with the appropriate V_t to provide the remaining face vertex vector V_f for each face ($V_f = V_t + \text{delta data}$). Rotation stage 62 provides the channel vectors V_c to projection stages 64 which project the three-dimensional V_c into two-dimensional display coordinates or vector V_d . Edge stage 65 provides a list of variable edges defined by the end points and the slope. The data flow through image processor 42 and the mode of operation thereof is controlled by processor control logic 70.

Texture stage 72 within the display generator 44 receives the visible edge list for coordination with the display raster. Deflection stage 74 provides the required analog deflection voltages to CRT display devices 82. Video stage 76 receives the color, intrinsic intensity and the size portion of the data for controlling the CRT beam voltage, current, and focus. Edge smoothing device 78 adjusts the rise time of the intensity data in response to the slope of each edge for dispersing the "staircase" along each edge into a lower resolution line. The CRT in device 82 may be a high resolution shadow-mask type cathode ray tube.

DETAILED DESCRIPTION OF INTERFACE CONTROLLER 46 AND THE DATA FORMAT

GP computer 40 has an in-core, buffer memory which accumulates blocks of image data required to form each display frame. The in-core buffer contains initialization points (V_o) and delta data from data base 48 plus each new position vector V_p and rotational matrix (H) as they are computed by flight computer 16.

The image data accumulating in the in-core buffer is periodically transferred as a data block to hardware RAM buffer 304 in interface controller 46. Controller 46 processes the data words sequentially to image processor 42 while GP computer 40 simultaneously assembles the next data block in the in-core buffer for the next data handshake with RAM 304. The accumulation of data blocks in GP computer 16 and the handshake data transfer to RAM 304 is outlined in the following four operations:

Operation I—Preflight Load—Data Base 48 to Core Memory

Prior to each training flight, the content of data base 48 is loaded into computer 40 core-memory. Image data from data base 40 includes sixteen control words (0000-1111) having bit formats as described hereinafter, initialization data V_o , delta data, etc.

Operation II—Aircraft Orientation Update

The in-core memory is updated periodically with the most recent aircraft orientation angles roll, pitch and yaw (H matrix data) from flight computer 16. Preferably, this aircraft update occurs once each frame. The H matrix data is received by computer 40 as the sine and cosine of each of the three orientation angles—six items of data. The software of computer 40 responds to the orientation data to form the rotational matrix H described in the specification. The software merely calculates the proper sine-cosine products to form a 3×3 matrix for each angle, and multiplies the three 3×3 matrices together to generate the nine elements of the rotational matrix H . These nine elements are generated each frame and inserted into RAM 304 at the proper place. The nine elements of rotational matrix H preferably occupy the lead position in the core-memory because the rotational perspective must be developed by rotation stage 62 each frame prior to displaying any of the object faces on display 82.

Operation III—Aircraft Position Update

The core-memory update also includes the most recent aircraft position vector V_p which latter forms a series of translated vectors V_t in translation stage 60.

Operation IV—Handshake Between Core-Memory and RAM 304

As required the contents of the core-memory matrix are serially transferred to RAM 304 in interface controller 46, starting with the nine rotational elements.

The four above described operations involve simple software steps. Operations I, III, and IV are merely data transfer steps. Operation II involves forming a triple 3×3 matrix product, a mathematical operation which is well understood. Subroutines are available to execute this systematic multiplication.

FORMAT SUMMARY

The data format is formed by groups of data words which describe the nature and position of each object feature, and spaced instruction words for identifying the type of data in the immediately subsequent group of data words. The MSB bits of each instruction word are coded to define the particular instruction contained in the word, and the remaining bits concern the subsequent data. In the embodiment shown, a sixteen bit format is employed. The four MSB define the instruction and are decoded by processor control logic 70 to control the flow of data through image processor 42. The four LSB of each instruction word reveal the number of subsequent data words in the data word group to be processed under that instruction word. Each instruction word is loaded into registers 310A and 310B by control logic 70 in due course, and the immediately subsequent group of data words is loaded into RAM 350.

FIVE LOAD INSTRUCTIONS (0-4)

Each load instruction transfers point coordinates from buffer 306 into RAM 350 as follows:

LDA (4)	15	12 11	8 7 6	3	0
	0 1 0 0	A A A A	R R	B B B B	

Load ALL instruction causes the subsequent group of B sets of X, Y, Z coordinates to be stored in RAM's 350X, 350Y, and 350Z, beginning at address A. The first coordinate (one of two sixteen bit words) is stored in the RAM 350X, the second in the RAM 350Y, and the third in the RAM 350Z. This sequence is repeated until B sets of coordinates have been loaded starting at address A. R specifies the significance of the bits in the subsequent sixteen bit data words for coordinating the distribution thereof across the 24 bits of RAM's 350.

Normal 24 bit resolution (R=3) requires two subsequent data words. The first word provides the sixteen LSB to RAM's 350 and the second word provides the 8MSB to RAM's 350. Vp and Vo data require the full 24 bits and therefore are preceded by an LDA instruction word with R=3. The LSB of Vp preferably corresponds to $\frac{1}{8}$ of an inch to eliminate detectable jitter of the scene from frame to frame. A new Vp is calculated by FS computer 16 each frame, and the round-off error in the LSB of Vp causes the entire earth coordinate system to jump a ground distance equal to the LSB. This interframe displacement (motion resolution) is minimized and rendered indetectable to the pilot trainee by providing aircraft position vector (Vp) resolution at the $\frac{1}{8}$ inch level. The LSB of Vo is preferably small in order to accurately position detailed structure within a terrain feature (positional resolution). In the embodiment shown, Vo LSB also equals $\frac{1}{8}$ inch because image processor 42 is already required to handle the $\frac{1}{8}$ inch bit in order to prevent interframe displacement. That is, the position resolution may have the same value as the motion resolution as in the embodiment shown; but it is not required that the two resolutions be equal. However, a $\frac{1}{8}$ inch Vo position resolution permits moving objects such as other airplanes and ground vehicles to be viewed without interframe displacement. The MSB of both Vp and Vo is 262,144 feet forming a cubic gaming volume in data base 48 which is 262,144 feet on an edge.

Fine 16 bit resolution (R=1) requires a single subsequent 16 bit data word of delta data which is entered into the 16LSB of 24 bit RAM's 350 (bits 16-23 are loaded with the sign bit 15). The MSB corresponds to 1024 feet (when LSB= $\frac{1}{8}$ inch). The fine 16 bit resolution may be used to process the vertices of small terrain faces (largest dimension less than 1024 feet) which is associated with high resolution detailed structure.

Coarse 16 bit resolution (R=2) requires a single 16 bit subsequent data word of delta data which is entered into the 16 MSB of 24 bit RAM's 350 (bits 0-7 are loaded with "0"s). The MSB=262,144 feet and LSB=8 feet. The coarse 16 bit resolution may be used to process the vertices of large terrain faces in which the dimensions have been rounded off to multiples of eight feet. While the size resolution of these faces is eight feet, they are positioned with the same resolution as the associated Vo.

LXY (3)	15	12 11	8 7 6	3	0
	0 0 1 1	A A A A	R R	B B B B	

5 Load XY instruction causes the subsequent group of B pairs of X and Y coordinates to be stored in the RAM 350X and RAM 350Y, beginning at address A. "0"s are stored in the corresponding addresses of the RAM 350Z. The data format is one or two 16 bit words of X data followed by one or two words of Y data. This sequence is repeated until B pairs of X-Y coordinates have been loaded into RAM's 350X and 350Y. The R codes are the same as for LDA.

LDX (0)	15	12 11	8 7 6	3	0
	0 0 0 0	A A A A	R R	B B B B	

10 Load X instruction causes the subsequent group of B X coordinates to be stored in the XT RAM 350X beginning at address A. Zeros are stored in the corresponding addresses of RAM's 350Y and 350Z.

LDY (1)	15	12 11	8 7 6	3	0
	0 0 0 1	A A A A	R R	B B B B	

15 Load Y instruction is the same as LDX except that the data is stored in RAM 350Y and "0"s are stored in the corresponding addresses in RAM 350X and RAM 350Z.

LDZ (2)	15	12 11	8 7 6	3	0
	0 0 1 0	A A A A	R R	B B B B	

20 Load Z instruction is the same as LDX except that the data is stored in the RAM 350Z and "0"s are stored in corresponding addresses of RAM's 350X and 350Y.

FIVE RECALL INSTRUCTIONS (5-9)

Recall instructions load the first vertice Vo of each face into RAM's 350 and initiates generation of the associated face.

RCA (9)	15	11	8 7 6	4	3	0
	1 0 0 1	A A A A	R S S S	B B B B		

25 Recall ALL instruction causes the single subsequent set of coordinates for the first vertice of a face, which typically is also an initialization vector Vo, to be loaded into the first location of RAM 350X, RAM 350Y, and 350Z. The other vertices of the current face have already been entered into RAM's 350 in CCW order as 16 bit coarse or fine data under one of the load instructions (0-4). These other B vertices are now recalled in CCW order from RAM's 350 beginning with address A of RCA. Normal 24 bit resolution (R=3) and coarse 16 bit resolution (R=2) have been previously described. S is a scale factor. When S=7, the current face is displayed full size. As S decreases the size of the current face is reduced by factors of 2.

RXY (8)	15	12 11	8 7 6	4	3	0
	1 0 0 0	A A A A	R S S S	B B B B		

30 Recall XY instruction causes the single subsequent set of first vertices Vo coordinates to be loaded into the first address of RAM 350X and then the first address of

RAM 310Y. RAM 350Z is unaffected. The face generation then proceeds as described under RCA.

RCX (5)

0	1	0	1	A	A	A	R	S	S	S	B	B	B
---	---	---	---	---	---	---	---	---	---	---	---	---	---

Recall X instruction causes the single subsequent X coordinate of the first vertice Vo to be loaded into the first address of RAM 350X. RAM's 350Y and 350Z are unaffected.

RCY (6)

0	1	1	0	A	A	A	R	S	S	S	B	B	B
---	---	---	---	---	---	---	---	---	---	---	---	---	---

Recall Y instruction causes the single subsequent Y coordinate of the first vertice Vo to be loaded into the first address of RAM 350Y; RAM's 350X and 350Y are unaffected.

RCZ (7)

0	1	1	1	A	A	A	R	S	S	S	B	B	B
---	---	---	---	---	---	---	---	---	---	---	---	---	---

Recall Z instruction causes the single subsequent Z coordinate of the first vertice Vo to be loaded into the first address of RAM 310Z; RAM's 350X and 350Y are unaffected.

RCL (10)

1	0	1	0	A	A	A	R	S	S	S	B	B	B
---	---	---	---	---	---	---	---	---	---	---	---	---	---

Recall Load instruction does not load any new data into RAM's 350 but is the same as RCX in other respects. RCL is used to hold the previous Vo in order to construct another face contiguous with or proximate to the previous face using the previous Vo as the first vertex or a landmark point for establishing the position of the vertices of the contiguous face.

OTHER INSTRUCTIONS

CIF (11)

15	12	11	10	9	8	4	3	0
1	0	1	1	SEL	AXIS	S±	IIII	B B B B

Color Intensity Flag instruction is followed by B additional words, i.e.,

CIF1(B = 1)

15	8	7	6	5	4	3	2	1	0
Spares	OBJ	CODE	FB	IOS	VER	RES			

CIF2(B = 2)

15	10	9	4	3	2	1	0
Color-	Color+	Col Sel	Spares				

which define the visual characteristics of each data base feature (face, line, or point). The visual characteristic of certain cultural objects such as signal beacons and runway lamps are a function of viewing direction and require directional data. SEL AXIS identifies the viewing axis to which the CIF data pertains:

SEL AXIS=00: the color and intensity of the object is uniform in all directions—ordinary object.

SEL AXIS=01: the color of the object depends on the direction of viewing along the X axis—bidirectional object.

SEL AXIS=10: bidirectional along Y axis.

SEL AXIS=11: bidirectional along Z axis.

S± (SIGN±) identifies the direction of view of the object along the axis identified by SEL AXIS. COLOR+ identifies the color of the object when

viewed from the S+ direction, and COLOR- identifies the color of the object when viewed from the S- direction. COL SEL permits ordinary non-direction features to be displayed in a color from COLOR+ (COL SEL=0) or from COLOR- (COL SEL=1). I (INTENSITY) determines the intensity of the data base feature. When only an intensity change is required to display the current object, only CIFO (B=0) is employed. OBJ CODE identifies the type of object to be recalled:

OBJ CODE = 000: 3 dimensional face (a face having a vertical component). Most 3D faces form part of a 3 dimensional object such as the side or top of a building. = 001: Spare. = 010: Spare. = 011: Face to line, such as runway stripes which narrow down to a line with distance. = 100: Sky. = 101: Line. = 110: Light point. = 111: 2 dimensional face, a completely horizontal face in the X-Y plane.
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The use of Recall instruction as illustrated in FIG. 2a is different for two dimensional faces on the X-Y ground plane (which always face the observer) and faces of a 3 dimensional object (which are sometimes occluded), as illustrated in FIG. 2. Two dimensional

faces are identified by a 2D face object code in the previously loaded CIFI data. RCX computes the vertices of each face by starting with the X, Y, Z coordinates of Vo stored in the first address of RAM's 350 and combining additional vector coordinates from RAM's 350 starting at address A. B is the number of vertices in the face, and, since Vo is the first vertex, B-1 additional vectors (Delta V1, Delta V2, . . . Delta VB-1) are required to generate the other vertices. The vertices are always stored and retrieved in counter-clockwise order.

Three dimensional faces are identified by a 3D object code. Vo is not used as a vertex for 3D faces, so that B additional vectors (Delta V1, Delta V2, . . . Delta VB) are required to display a face having B vertices. The RAM addresses containing the additional vector coordinates for 3D faces are provided by one or two data words 3DV1 and 3DV2 following the X data word or words. Each additional vector in 3D recall describes the position of a vertex with respect to Vo as opposed to a 2D recall, in which each additional vector describes

the position of a vertex with respect to the previous vertex. The address format for additional 3D vectors in RAM 350 is

55 V1

15	VR	VR	VR	VR	0
D D D D	C C C C	B B B B	A A A A		first word

 V2

15	VR	VR	VR	VR	0
H H H	G G G G	F F F F	E E E E		second word

60 If the face has four or fewer vertices, only the first word is used. The order in which the RAM 350 addresses are used is reverse alphabetical. For example, when recalling a face having five vertices, the first vertex will be

65 computed using the vector stored at E. The last vertex is always stored at A. A in the RCX instruction is also the address of the normal vector stored in normal RAM 440N. The normal vector is used to test the visibility of

a face and must have been previously loaded in normal RAM 440N using a LDN instruction (described herein-after). Scale factor is the same for a 3D face as for a 2D face.

FB identifies data fed back for CRT correction to 5 eliminate ballistic nonlinearities and provide a true display.

IOS identifies data displayed on the instructor's monitor 28 only.

VER RES determines the scan line density (vertical 10 display resolution in horizontal lines per vertical scan).

VER RES = 000: 128 lines low resolution for rapidly painting structureless large areas such as the sky with a defocused electron beam.

- = 001: 256
- = 010: 384
- = 011: 512
- = 100: 640
- = 101: 768
- = 110: 896
- = 111: 1024 lines high resolution for painting detailed objects.

LCD (15)

15	12	11	8	7	0
1	1	1	1		C C C C C C C C

Load Correct Data instruction enters C vertices with corrected CRT coordinates.

STG (12)

15	11 0 0	A A A A	C C C C C C C C
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Control String instruction causes the display of string of C equally spaced lights or four-sided two dimensional faces, depending on the CIF1 OBJ CODE. The first light of a string is displayed at the Vo+A position and a spacing vector stored at A+1 is used to fix the position of the second light and all successive lights until C lights have been displayed. The first vertex of the first face of a string of faces is displayed at the Vi+A position and the other three vertices are found successively adding the vectors stored at RAM's 350 addresses A+1, A+2, and A+3. The vector stored at A+4 locates the first vertex of the next face with respect to the last vertex of the current face.

LDH (13)

15	12	8	7	6	5	4	3	0
1	1	0	1	A	A	A	0	C C B B B B

Control Load H instruction loads the H rotation matrix on data bus 307 into RAM 410H in rotation stage 62. The elements of the rotation matrix are in 16 bit 2's complement form, and each address of RAM 410H will store three elements. The rotation matrix multiplies the translated X, Y, and Z coordinates in the following form:

$$\begin{bmatrix} h_{11} & h_{12} & h_{13} \\ h_{21} & h_{22} & h_{23} \\ h_{31} & h_{32} & h_{33} \end{bmatrix} \begin{bmatrix} XT \\ YT \\ ZT \end{bmatrix} = \begin{bmatrix} XR \\ YR \\ ZR \end{bmatrix} = \begin{aligned} & h_{11} XT + h_{12} YT + h_{13} ZT \\ & h_{21} XT + h_{22} YT + h_{23} ZT \\ & h_{31} XT + h_{32} YT + h_{33} ZT \end{aligned}$$

The element data follows the LDH instruction in the following order:

h31, h32, h33, h21, h22, h23, h11, h12, h13.

The matrix is always stored in the first three addresses of RAM 410H, so A=0, the initial address and B=3, the number of matrix rows. C is the channel number associated with rotation matrix.

LDN (14)

15	12	11	8	7	6	3	0				
1	1	0	1	A	A	A	1	B	B	B	B

Control Load N instruction loads B face normal vectors on data bus 307 into normal vector RAM 440N in rotation stage 62, starting at address A. Each vector consists of three 16 bit data words in order Nx, Ny, Nz. The Control Load N will therefore always be followed by three B words of data. Each address in normal RAM 410N is associated with a three dimensional face of identical address in RAM's 350. Both RAM's are addressed during the Control Recall of a 3D face.

DETAILED DESCRIPTION OF DIGITAL VISUAL COMPUTER 12

Each stage of digital visual system 12 is shown in detail in FIGS. 3 through 9. Preferred embodiments are disclosed at the detailed logic level. Each component is described by function, input-output characters, or conventional nomenclature to enable one skilled in the arts of simulation, digital design, and computer programming to practice the invention. The components are additionally designated by the manufacturer's IC type number from the following integrated circuits data books:

Texas Instruments Incorporated
"The TTL Data Book of Design Engineers"
First Edition, Copyright 1973

National Semiconductor Corporation
"Digital Integrated Circuits"
January 1974

Advanced Micro Devices Inc.
"Advanced Micro Devices Data Book"
Copyright 1974

unless otherwise specified. Further, many inverters are employed throughout CDIG system 10 for buffering signals with multiple loads. These buffer inverters are type 74SO4 unless otherwise stated.

TRANSLATION STAGE 60

General Operation

FIG. 3 shows translation stage 60 of image processor 42 and a portion of controller 46. Controller 46 receives image data in sequential order from computer 40 at input 302 of random access memory 304. The image data is arranged in data blocks M bits wide and N words long, which in the embodiment shown is 16×1024. RAM 304 periodically handshakes with a core memory in GP computer 40 to reproduce each block of data. Image data is sequentially transferred from RAM 304

through a buffer register 306 to image data bus 307 in response to load pulses from interface controller 46.

Each instruction word on bus 307 is loaded into instruction registers 310 A and B which forwards the code bits (four MSB's) to control logic 70. Control logic 70 then selectively activates the remaining blocks of translation stage 60 for processing the subsequent B words of data appropriately. Load instructions (0-4) cause control logic 70 to send WRITE to RAM's 350, which then writes the subsequent B data words starting at ADDRESS A. Counter 320A increments ADDRESS A while counter 320B decrements down from B. When the B count expires, B=0 is forwarded to logic 70 and the next instruction is loaded into instruction registers 310.

V_p is loaded into RAM's 350 by a Load A instruction (R=3) immediately after each handshake, and V_p is always positioned at the same address (address 1). Next, B words of delta data vectors is entered by another load instruction.

Recall instructions (5-9) load the V_o associated with the previously loaded B words of delta data. Each V_o is positioned at the same address in RAM 350 (address 0). The recall instruction causes control logic 70 to forward READ to RAM's 350, and the B words of delta delta are recalled from RAM's 350 and processed through the remainder of translation stage 60.

CIF instruction causes control logic 70 to forward LOAD to CIF register 330 to receive SEL AXIS, SIGN_±, and Intensity data from instruction registers 310. B subsequent data words are entered into CIF-1 register 331 and CIF-2 register 332 where the CIF data is temporarily held. The CIF data is advanced into corresponding CIF registers 460 in rotation stage 62 as V_f data enters rotation stage 62 from normalization register 380.

Three dimensional vertex registers 341 and 342 receive the addresses of vertices of 3D faces in RAM 350. The addresses in registers 341 and 342 address RAM's 350 via address counter 320A.

RAM's 350 write image data from interface controller 46 after load instructions and read image data after recall instructions. RAM's 350 temporarily store V_p and delta V's until the associated V_o is entered permitting the faces to be generated.

Scalers 360 (X, Y, and Z) control the size of the displayed image by expanding or contracting the X, Y, and Z position coordinates by factors of two. S data from register 310B shifts the binary decimal point to effect the scaling.

Accumulators 370 receive the X, Y, and Z position coordinates and perform the following translation computations (illustrated in FIG. 2):

basic translation: from the origin 210 of data base coordinate system to the origin 220 of aircraft 14 coordinate system

$$V_p + V_o = V_t$$

2D translation: from initial vertex to the remaining vertices sequentially—cumulative (landing strip 230)

$$V_t + \text{Delta } V_1 = V_{t1}$$

$$V_{t1} + \text{Delta } V_2 = V_{t2}$$

$$V_{tn} + \text{Delta } (V_{n+1}) = V_{(tn+1)}$$

3D translation: from initial vertex to each remaining vertex separately—non cumulative (hanger 240)

$$V_t + \text{Delta } V_1 = V_{t1}$$

$$V_t + \text{Delta } V_n = V_{tn}$$

5 Normalization registers 380 (X, Y, and Z) loads the translated vertices V_t, and left shifts leading zeros (or ones for negative V_t's) in response to control logic 70. The first difference between the MSB and the second 10 MSB in any of the normalization registers 380 generates a normalization complete signal, (NCS), back to control logic 70. Normalization complete in any of the normalization registers 380 stops the normalization process of all the registers insuring that the normalized points 15 maintain consistent dimension units and remain on the same line of vision as viewed on display 82. Normalization has the advantage of reducing the 24 bit input image data into bits of normalized image data by eliminating either leading zeros (or ones for negative numbers). The data load is reduced to 66% with negligible loss in position resolution.

DETAILED DESCRIPTION

25 RAM 304 may be formed by a 16 bit \times 24 word RAM (sixteen 93415's, Fairchild) for holding the block of image data from GP computer 40.

Buffer register 306 may be formed by a 16 bit register (four 74S175's) followed by buffer inverters as required (74S04).

30 Register 310A may be an eight bit register (two 74S175's) for receiving four bits of code (4MSB) and four bits of RAM address (4LSB).

Register 310B and word counter 320B may be formed together by an eight bit down counter (two 74S163) for receiving the compliment of B and counting to 15. At B compliment=15, B=0 appears on the carry out terminal.

35 Address counter 320A may be a 2:1 inverting multiplexer (74S158) followed by a four bit up counter (one 74S163). During load and recall instructions, counter 320A increments the start address AAAA to RAM's 350. While processing three dimensional faces counter 320A processes the face vertex addresses in three D registers 341 and 342.

40 CIF register 330 may be an eight bit register (two 74S175) for receiving eight bits of SEL AXIS, S_± and Intensity Data from the CIF Load instruction.

45 CIF-1 and CIF-2 registers 331 and 332 may be 16 bit registers (four 74S174) for receiving two 16 bit words of CIF data immediately following the CIF instruction.

Three dimensional registers 341 and 342 may be eight 50 4 bit tristate registers (eight 8551) preceded by a 3 line to 8 line decoder (one half 74S139) which enables one of the eight tristate registers in response to the three LSB's of B from word counter 320B.

55 RAM 350X may be a 24 bit RAM (six 74S189's) to accomodate the 24 bits of X coordinate image data. The 24 bit RAM is preceded by a 2:1 8 bit multiplexer (two 74S158) between a pair of true compliment zero one elements (two 74H87's each). During 16 bit fine resolution (R=1) the right hand zero one element forwards the 8LSB's of the image data to the 24 bit RAM, and the righthand zero one element enters all zeros (or all ones 60 depending on the sign of the image data). During 16 bit coarse resolution (R=2) the right hand zero one element enters all zeros and the lefthand zero one element forwards the 8 MSB's.

Scaler 360x may be formed by a flow through right shifter device (twelve 25S10's AMD) in response to S data from register 310B counter.

Accumulator 370x may be a 24 bit adder (six 74283's) for receiving data at the A input, followed by a 24 bit return register (six 74S175's) which outputs to the B input. Vp is processed through the adder and return register, and returned to the B input. Vo is loaded at the A input and added to Vp to form Vt and returned to the B input. Delta data is then loaded at the A input and added to Vt to form the remaining vertex vectors Vfl-Vfn, which are advanced through the return register to a 24 bit buffer register (four 74S174's) where the Vfs are held until normalizer 380x is free.

Normalizer 380x may be formed by a 24 bit shift register (three 74199) plus a Buffer register (four 74S174's) which holds the normalized Vf's until rotation stage 62 is free to handle the next Vf.

ROTATION STAGE 62

General-H Matrix

FIG. 4 shows rotation stage 62 of image processor 42 which multiplies the translated point vectors Vfl-Vfn from translation stage 60 by the rotation matrix H provided on data bus 307 to produce a rotated or channel vectors Vc (XcYcZc):

$$\begin{array}{l} Xc \\ Yc = [H] Yf \\ Zc \end{array}$$

Each channel corresponds to the perspective view from one window of aircraft 14.

The rotation matrix H is developed from yaw (Y, left), pitch (P, down), and roll (R, right) motions by flight simulator 16 using conventional software. The order of rotation is Y followed by P, and the matrices for the separate rotations from translated to rotated pilot eye or channel coordinates are as follows:

$$\begin{aligned} HY &= \begin{bmatrix} \cos Y & \sin Y & 0 \\ -\sin Y & \cos Y & 0 \\ 0 & 0 & 1 \end{bmatrix} \\ HP &= \begin{bmatrix} \cos P & 0 & -\sin P \\ 0 & 1 & 0 \\ \sin P & 0 & \cos P \end{bmatrix} \\ HR &= \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos R & \sin R \\ 0 & -\sin R & \cos R \end{bmatrix} \end{aligned}$$

The composite matrix H describing this rotation is given by the matrix product:

$$[H] = [HR][HP][HY] = 3 \text{ columns} \times 3 \text{ rows matrix}$$

The aircraft attitude matrix H is constant for each frame and is therefore computed only once per frame for each channel.

The three elements of the first column of the H matrix are entered into H RAM 410x by WRITE from control logic 70 immediately subsequent to the Load H instruction. The first column is then multiplied by the Xf coordinate of each of the translated vector series Vfl-Vfn in turn within column multiplier 420X. The three elements of the second and third columns of [H] are similarly entered into H RAM 410Y and 410Z (not shown). The

nine products generated above are combined into Xc, Yc, and Zc by row multiplexer 424 and adder 430. The resulting Vc is forwarded to clipping stage 63.

GENERAL-VISIBILITY TEST

The rotation circuitry also provides the multiplication for the dot product visibility test for the faces which form three dimensional structures such as buildings:

$$Vt \cdot Vn = M \cos P$$

where:

Vt is the translated vector extending from aircraft 14 to the first vertex of the face being tested; and

Vn is the vector normal to the face being tested.

When cos P is negative, P is greater than 90° and the face is visible because the face is on the front or exposed side of the building. When cos P is positive, P is less than 90° and the face is invisible because the face is on the back side of the building. The sign bit of the dot product is employed for back side elimination, a simple occulting technique.

The Xn, Yn, and Zn coordinates of Vn are entered into N RAM's 410X, Y and Z respectively immediately subsequent to the Load N instruction. Each coordinate is multiplied by the corresponding coordinate Xt, Yt, and Zt of Vt in multipliers 420 and the sign bit of the resulting quantity is forwarded to control logic 70.

DETAILED DESCRIPTION

H RAM 410x may be a 16 word by 16 bit sequential access memory (for 74S189's) for holding the three words in the first column of the 3×3 H matrix and providing 13 spare 16 bit addresses. WRITE and ADDRESS are provided by control logic 70.

N RAM 410x may be a 16 word by 16 bit random access memory (four 74S189's) for holding up to sixteen words of Xn which accommodates a three dimensional complex structure with up to sixteen faces.

Multiplicand register 414x may be a 16 bit buffer register (four 74S175's) for holding the current output of H and N RAM's 410x available to multiplexer 420x while the next address in RAM's 410x are accessed.

MUX 416x may be a 16 bit dual 4-1 multiplexer (three 74S153's) for providing four bits of output plus carry over bit.

Multiplier register 418x may be a 5 bit buffer register (one 74S174) for holding the output of MUX 416x available to multiplier 420x.

Column multiplier 420x may be formed by eight AM 25S05's (Advanced Micro Devices in 16 bit×4 bit configuration) followed by a buffer product register (three 74S175's) and operates as described in connection with Multiplier 330 in U.S. Pat. No. 3,996,672 which issued Dec. 14, 1976.

Row Multiplexer 424 may be a 20 bit 4 to 1 multiplexer (ten 74157's connected in parallel) which sequentially select the first row elements of each column for summing in row adder 430 to form Xc. The second and third row elements are likewise summed to provide Yc and Zc.

Row adder 430 may be a 20 bit adder (five 74783's) for summing the row products of the H matrix.

Accumulator 440 (three 74174's) returns intermediate sums to multiplexer 440 which are required to forming Vc.

Buffer registers 450 may be 18 bit registers (four 74175's) for holding Vc (Vx, Vy, Vz) prior to clipping.

CIF register 460 may be a 40 bit register for holding the CIF data from CIF registers 330, 331, and 332.

CLIPPING STAGE 63

General

FIG. 5 shows clipping stage 63 which eliminates points outside the viewing volume or pyramid of vision 250 shown in FIG. 2a. Pyramid of vision 250 has its vertex at the eye of the pilot (origin 220). The viewing volume in the embodiment shown is four sided, bounded by four planes defined by the four sides of the aircraft window.

Clipping is accomplished at the object face level. Vertices defining each face edge are processed in sequence through clipping stage 63 to determine whether the face is:

- Case A—face completely within view,
- Case B—face partially within view, or
- Case C—face completely out of view.

Faces which are only partially in view (Case B) are intercepted by the sides of pyramid of vision 250. In the process of clipping, Case B faces are modified by the addition of new edges. The result is a modified closed polygon face that is completely within pyramid 250.

The position of any point or vertex relative to pyramid of vision 250 is defined by the distance of that vertex from each of the four sides of pyramid of vision 250. Referring to FIG. 2a point 254 forming the top of the flag pole 256 is positionally defined by the four window coordinates vl, vr, vb, vt in Zc plane 260. These window coordinates are calculated as follows:

$$\begin{aligned} vl &= K_l Z + X \\ vr &= K_r Z - X \\ vb &= K_b Z + Y \\ vt &= K_t Z - Y \end{aligned}$$

where the K's are constants associated with the vertex angles of pyramid 250. For a square pyramid of vision having equal vertex angles A, $K_l = K_r = K_b = K_t = \tan(A/2)$. A point is inside the truncated pyramid of vision 250 if $vl \geq 0, vr \geq 0, vb \geq 0, vt \geq 0$, and $Zc > 0$.

The above window coordinates are calculated from Vc by window logic circuits 510-l, 510-r, 510-b, 510-t, and 510-z shown in FIG. 5 (only 510-l is shown in detail). Window circuit 510-1 receives Xc and Zc from 1:r multiplexer 520 for temporary storage in interior working registers 530. Adder 540 and inverter 544 cooperate to perform the required addition. Window coordinates vl and vt are forwarded to projection stage 64 to become display coordinates Xd and Yd, and Zc is forwarded for range attenuation effects.

The signs of the window coordinates are combined in a single five-bit out-code (OC):

$$OC = \text{sign } l, \text{ sign } r, \text{ sign } b, \text{ sign } t \text{ (and sign } Z\text{)}$$

where the sign of each window coordinate is "0" for positive and "1" for negative. The origin of each window coordinate is the corresponding boundary of image window 262 with the negative direction extending away from image window 262 (see FIG. 2b, left for vl, right for vr, down for vb, and up for vt). The positive direction for each window coordinate is toward the

center of image window 262. The four boundaries of pyramid 260 subdivide the positive half-space in front of aircraft 14 into nine regions. The out-code of each Vc identifies the region in which the point or vertex is located. The out-code for each region of the two-dimensional projection of pyramid 250 is shown in the following table:

	upper left region	upper visible region	upper right region
10	1001 (0)	0001 (0)	0101 (0)
15	1000 (0)	0000 (0)	0100 (0)
20	lower left region	lower visible region	lower right region
	1010 (0)	0010 (0)	0110 (0)

The relative position of any face edge to pyramid 250 can be found by examining the outcodes of the end points of the edge. If both vertices are behind the $Z_c=0$ plane (that is behind the pilot's eye where Z_c is negative), the sign $Z(1)=\text{sign } Z(2)=1$ and the face edge is not visible and can be rejected. If both vertices are in front of the $Z_c=0$ plane (in front of the pilot's eye where Z_c is positive), then $\text{sign } Z(1)=\text{sign } Z(2)=0$. If the face edge intersects the $Z_c=0$ plane, then $\text{sign } Z_1 \neq \text{sign } Z_2$. The intersection is found and only the portion of the edge extending in front of the pilot's eye need be considered.

Three further possibilities for the relative position of a face edge with respect to pyramid 250:

Case 1: Both ends of the face edge are within view. No clipping is necessary: $OC(1)=0000(0), OC(2)=0000(0)$.

Case 2: One end of the face edge is within view and the other end is outside. The face edge intersects pyramid 250: $OC(1)=0000(0)$ and $OC(2) \neq 0000(0)$ or $OC(1) \neq 0000(0)$ and $OC(2)=0000(0)$.

Case 3: Both ends are outside pyramid of vision 250: $OC(1) \neq 0000(0)$ and $OC(2) \neq 0000(0)$.

In Case 3, definite decisions can be made only if the end points of the edge are either both to the right or both to the left ($\text{sign } l(1)=\text{sign } l(2)=1$ (negative) or $\text{sign } r(1)=\text{sign } r(2)=1$ (negative)). Furthermore, if $OC(1)=OC(2) \neq 0000$, both ends are outside, in the same region. In all these cases the face edge can be rejected. The rejection criteria can be expressed as a Boolean function (R) of the two out-codes. If $R=0$, none of the above rejection criteria are satisfied, and a part of the face edge boundary may go through image window 260.

Whenever Case 2 is found in the clipping process, the intersection of each face edge and pyramid of vision 250 is determined by window circuits 510 and the clipping portion of control 70 using a binary search technique. The algorithm for the search is as follows:

- (A) Let the window coordinates of the vertex inside image window 260 be V_{in} and the outside coordinates be V_{out} .
- (B) The midpoint between V_{in} and V_{out} is calculated.
- (C) If the midpoint is within pyramid 250, V_{in} is replaced by the midpoint.

- (D) If the midpoint is outside, Vout is replaced by the midpoint.
 (E) The process continues until the distance of the midpoint from one side of pyramid 250 is less than the termination tolerance.

There remains the problem of modifying the edges of clipped faces. In some situations the intersections of the face edges and pyramid of vision 250 define the new face edge. In other situations one or more corners of the window must be inserted into the sequence of vertices to complete the closed polygon face.

In a special case all vertices are outside pyramid 250 and the edges do not intersect pyramid 250. There remains ambiguity as to whether the face is within view. Referring to FIG. 2b showing image window 262, 4 rays (R1, R2, R3, and R4) extend from the four corners (C1, C2, C3, and C4) of window 260. If a ray is intersected an odd number of times by the edges of the polygon face, then the corresponding corner is surrounded by the polygon. This technique can be implemented by inspecting the out-codes of the adjacent vertices defining each edge. The criterion for crossing the rays is very similar to the rejection criterion and is obtained by logical operations. As an example, R1 is crossed if sign t(1)=sign t(2)=1 and sign l(1)≠sign l(2).

PROJECTION STAGE 64

General

FIG. 6 shows projection and clipping stage 64 of image processor 42 which projects three-dimensional window coordinates v1, vt, and Vz from clipping stage 63 into a two-dimensional vector Vd (Xd, Yd). The projected vectors Vd define the end points of each face edge for face generation stage 65. The projection is accomplished by dividing v1 and vt by Zc through a binary division nonrestoring technique (described in "Digital Arithmetic-I" by Y. Chu pages 39-43). Z/2 registers 610-l and 610-t load the divisor Zc/2, and MUX/Register 620-l and 620-t select and load the dividend v1/2 and vt/2 in response to control logic 70. The inputs to registers 610 and 620 are right-shifted by one digit to establish the division by two. Arithmetic logic unit ALU 630-l and 630-t then receive the dividends through shift return loops 623-l and 623-t, or subtract Zc/2 thereto in response to a ±function from logic 70. The dividend $\pm Zc/2$ term is loaded into MUX 620, returned to ALU's 630, and then combined with another $\pm Z/2$. The output of ALU's is slew wired with respect to the input of MUX's 620 causing a division by two right shift. The v1/Vz and vt/Vz quotients are generated one bit at a time, MSB first, by comparing the sign bit (MSB) of Zc with the sign bit of the partial remainders with MUX 620 through sign gates 636-l and 636-t. The quotient bits individually enter quotient registers 640-l and 640-t, and are left-shifted by control logic 70. Zc on line 592 from range register 590 is loaded into renormalization register 650 and right-shifted by control logic 708 the same number of places as were left-shifted in normalizer 370 in translation stage 60. Color, intensity, and flag data on line 592 from CIF register 590 is loaded into CIF register 660 in response to control logic 70.

DETAILED DESCRIPTION

Z/2 register 610 may be a 24 bit register (four 74S174's).

MUX/Registers 620 may be 24 bit 2:1 multiplexers (five 74S298's) with storage.

ALU's 630 may be 16 bit flowthrough arithmetic logic units (four 74S181's + one 74S182).

Sign gates 636 may be exclusive OR gates (74S86).

Quotient registers 640 may be 12 bit shift registers (three 74164's) for receiving the projected data Xd and Yd one bit at a time as it is generated by ALU's 630.

Zc register 650 may be a 24 bit shift register (six 74S195's).

CIF register 660 may be a series of 74S174's.

EDGE STAGE 65

General

FIG. 7 shows edge stage 65 having Xd processor 706X and Yd processor 706Y which receive projected face vertex coordinates (Xd and Yd) from projection stage 64 and provides face edge lists to display generator 44. Each edge is defined by edge data including a starting point (Xds, Yds), the Y coordinate of the termination point (Ydt), plus the slope of the edge (delta X/delta Y).

The Y coordinates of each set of face vertices (Xd and Yd) are loaded into current Y mux-register 710 and advanced to previous Y register 716 in CCW order as defined in data base 48. Each current Y coordinate (Ydc) and previous Y coordinate (Ydp) are forwarded to adder 720 for calculating a delta Y for each face edge or pair of points (delta Y = Ydc - Ydp). Simultaneously, each Ydc and Ydp are entered into Y start multiplexer 730s and Y terminate multiplexer 730t. The starting Y coordinate Yds is the end point of each face edge that is scanned first on CRT 82; and the terminate Y coordinate Ydt is scanned last. In the embodiment shown, the conventional top to bottom scan is employed. Therefore, the start point Yds is always the smaller of the two adjacent points Ydc and Ydp. The sign bit of delta Y (SIGN ΔY) defines which is smaller, Ydc or Ydp, as follows:

for + delta Y	for - delta Y
Ydc = Ydt, and Xdc = Xdt	Ydc = Yds, and Xdc = Xds
Ydp = Yds, and Xdp = Xds	Xdp = Xdt, and Xdp = Xdt

and activates multiplexers 730s and 730t accordingly. Slope divider 740 provides the slope of each edge face by computing delta X/delta Y for the corresponding pair of vertices.

The face edges are arranged in scan order by Yds sorter 750 according to the smallest Yds. Each edge data set is loaded into sorter 750 in CCW order and forwarded to image generator 44 in order of smallest Yds for accomodating the top to bottom scan.

DETAILED DESCRIPTION

Xd processor 706X has the same hardware as Yd processor 706Y, and is therefore not shown in detail.

Current Y mux-register 710 may be a 12 bit 2:1 multiplexer-register (three 74298's) for the current vertex of each face as the vertices are received in CCW order from quotient registers 640-l and 640-t.

Previous Y register 716 may be a 12 bit storage register (two 74174's) for holding the vertex just preceding the current vertex.

First vertex Y register 718 may be a 12 bit storage register (two 74174's) for holding the first vertex while the intermediate vertices are processed. The first vertex

is loaded into current mux-register 710 as the last vertex is advanced to previous vertex status to form the last edge of the face.

Adder 720 may be a 12 bit adder (three 74283's) for calculating delts $Y = Ydc - Ydp$, and forwarding SIGN 5 Y to Y and X multiplexers-registers 730s and 730t.

Inverter 722 may be a 12 bit inverting buffer (two 74S04's) for inverting Ydp into $-Ydp$. The carry in on adder 720 is forced to 1 to complete the complement of Ydp .

Start point and terminate point multiplexer-register 730 may be 12 bit 2:1 multiplexer-registers (three 74298's each) for simultaneously holding both Ydc and Ydp available for selection as either Yds or Ydt .

Delta Y register 724 may be a 12 bit storage register 15 (three 74S175's) for holding delta Yc while divider 740 forms the slope (delta Xp /delta Yp) for the previous edge. Additionally register 724 may include a zero detect circuit (one 74S30) for providing delta $Y=0$ to control 70 when the slope is horizontal and the edge 20 may be omitted from further processing.

Divider 740 may be a 12 input bit-20 output bit binary division nonrestoring divider as described in projection stage 64, for calculating slope=delta X /delta Y . The dividend delta X may be right shifted into additional 25 shift register (one 74166) for scaling down the resulting slope to accomodate a Y increment of one raster line. In the embodiment shown the right shift is nine places to accomodate a 1024 scan line, interlaced display (2 to the 9th=512).

Sorter 750 may be a 12 bit key-96 bit non key sorter for output edge data in order ascending of Yds , formed by:

- (a) a 16 word 12 bit key data RAM (three 74S189's) for receiving and storing the key data (Yds) in 35 input order.

- (b) a 16 word 5 bit pointer RAM (two 74S189's) for storing the RAM pointers.
- (c) a three level pointer pushdown stock (two mux-registers 74298's—first level, one 74S174—second level, and one 74S174—third level) for manipulating pointers into sorted order each time a new key is received by the key data RAM.
- (d) address counter (one 74161) and smallest key pointer register (one 74S174) for generating RAM addresses and storing the current smallest key RAM address.
- (e) RAM address multiplexer (two 74S153's) and a pointer RAM input multiplexer (three 74S153's) which cooperates with the three level stack and address counter for selecting RAM addresses and the pointer RAM input.
- (f) an existing key register (three 74S175's) and comparator (three 74S85's) for determining where to insert the input key among the existing key in the key data RAM. The existing key register also stores key data to be advanced to image generator 44.
- (g) non key data output register (twenty-four 74S175's) for storing non key data (Xds , slope, Ydt , Zc , and CIF) to be advanced to image generator 44.

CONTROL LOGIC

Processor control logic 70 responds to instruction 30 code and data flags contained in the data flow from data base 48 for processing the coordinate data through image processor 42. The flow tables described below disclose the logic involved in controlling each stage of image processor 42. Various hardware circuit configurations could incorporate this logic.

TRANSLATION STAGE 60—CONTROL LOGIC FLOW TABLE

I. TRANSFER INSTRUCTION WORD:
CONTROLLER 46 TO REGISTER 310

STEP IA:	(1) Maintain LOAD signal on instruction register 310. (2) Load next instruction from buffer register 306 into instruction register 310 (LOAD).
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DECISION IA:	Is image data available to translation stage 60 on data bus 307? (DAV) <u>YES—STEP IB NO—STEP IA</u>
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STEP IB:	(1) Clear accumulator 370 (CLR). (2) Clear scaler data "S" from scale register in scaler 360. (3) Clear address counter 320A (CLR). (4) Set DAR from control logic 70, wait for DAV from interface controller 46.
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DECISION IB:	Decode four MSB of instruction in register 310A to identify one of sixteen instructions (0-15).
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II. LOAD X INSTRUCTION—LDX (0)

STEP IIA:	(1) Load address counter 320A with four bits of address "A" (LOAD). (2) Unit decrement word counter 320B (DEC).
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DECISION IIA:	DAV? <u>YES—DECISION IIB NO—DECISION IIA</u>
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DECISION IIB:	What is R? <table border="0"> <tr> <th>R = 1 (fine 16 bit)</th> <th>R = 2 (coarse 16 bit)</th> <th>R = 3 (normal 24 bit)</th> </tr> <tr> <td>1. Load 16 LSB from bus 307 into RAM 350X.</td> <td>1. Same as DECISION IIB (R = 1) 1 through 3 except load 16 MSB at 1.</td> <td>1. Load 16 LSB from bus 307 into RAM 350X. 2. Request DAR, wait for DAV.</td> </tr> <tr> <td>2. Load zeros</td> <td></td> <td></td> </tr> </table>	R = 1 (fine 16 bit)	R = 2 (coarse 16 bit)	R = 3 (normal 24 bit)	1. Load 16 LSB from bus 307 into RAM 350X.	1. Same as DECISION IIB (R = 1) 1 through 3 except load 16 MSB at 1.	1. Load 16 LSB from bus 307 into RAM 350X. 2. Request DAR, wait for DAV.	2. Load zeros		
R = 1 (fine 16 bit)	R = 2 (coarse 16 bit)	R = 3 (normal 24 bit)								
1. Load 16 LSB from bus 307 into RAM 350X.	1. Same as DECISION IIB (R = 1) 1 through 3 except load 16 MSB at 1.	1. Load 16 LSB from bus 307 into RAM 350X. 2. Request DAR, wait for DAV.								
2. Load zeros										

-continued

TRANSLATION STAGE 60—CONTROL LOGIC FLOW TABLE

into RAMs 350 Y and Z.		3. Load 8 MSB from bus 307 into RAM 350X.
3.a. Unit increment address counter 320A (INC).		4. Load zeros into RAMs 350 Y and Z.
3.b. Unit decrement word counter 320B (DEC).		5. Same as DECISION IIB (R = 1) 3.
3.c. Set DAR, wait for DAV.		
4. DECISION IIC.	2. DECISION IIC.	6. DECISION IIC.
DECISION IIIC: Is word count in register 320 B = 0? YES—STEP IA		NO—DECISION IIIA
III. LOAD Y INSTRUCTION—LDY (1)		
STEP IIIA: Same as STEP IIA.		
DECISION IIIA: DAV? YES—DECISION IIIB		NO—DECISION IIIA
DECISION IIIB: What is R? R = 1	R = 2	R = 3
1. Load 16 LSB from bus 307 into RAM 350Y. X and Z.	1. Same as DECISION IIIB (R = 1) 1 through 3 except load 16 MSB at 1.	1. Load 16 LSB from bus 307 into RAM 350Y. 2. Set DAR, wait for DAV. 3. Load 8 MSB from bus 307 into RAM 350X.
2. Load zeros into RAMs 350 X and Z.		4. Load zeros into RAMs 350 X and Z.
3. Same as DECISION IIB (R = 1) 3.		5. Same as DECISION IIB (R = 1) 3.
4. DECISION IIIIC.	2. DECISION IIIIC.	6. DECISION IIIIC.
DECISION IIIIC: Is word count in register 320 B = 0? YES—STEP IA		NO—DECISION IIIA
IV. LOAD Z INSTRUCTION—LDZ (2)		
STEP IVA: Same as STEP IIA.		
DECISION IVA: DAV? YES—DECISION IIB		NO—DECISION IVA
DECISION IVB: What is R? R = 1	R = 2	R = 3
1. Load 16 LSB from bus 307 into RAM 350Z. X and Y.	1. Same as DECISION IVB (R = 1) 1 through 3, except load 16 MSB at 1.	1. Load 16 LSB from bus 307 into RAM 350Z. 2. Set DAR, wait for DAV. 3. Load 8 MSB from bus 307 into RAM 350Z.
2. Load zeros into RAMs 350 X and Y.		4. Load zeros into RAMs 350 X and Y.
3. Same as DECISION II (R = 1) 3.		5. Same as DECISION IIB (R = 1) 3.
4. DECISION IVC.	2. DECISION IVC.	6. DECISION IVC.
DECISION IVC: Is word count in register 320 B = 0? YES—STEP IA		NO—DECISION IVA
V. LOAD XY INSTRUCTION—LXY (3)		
STEP VA: Same as STEP IIA.		
DECISION VA: DAV? YES—DECISION VB		NO—DECISION VA
DECISION VB: What is R? R = 1	R = 2	R = 3
1. Load 16 LSB from bus 307	1. Same as DECISION VB	1. Load 16 LSB from bus 307

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TRANSLATION STAGE 60—CONTROL LOGIC FLOW TABLE

into RAM 350X.	(R = 1) 1	into RAM 350X.
2. Set DAR, wait for DAV.	through 5, ex- cept load 16	2. Set DAR, wait for DAV.
3. Load 16 LSB from bus 307	MSB at 1 and 3.	3. Load 8 MSB from bus 307
into RAM 350Y.	.	into RAM 350X.
4. Load zeros	.	4. Set DAR, wait for DAV.
into RAM 350Z.	.	5. Load 16 LSB from bus 307
5. Same as DE- CISION IIB (R = 1) 3.	.	into RAM 350Y.
.	.	6. Set DAR, wait for DAV.
.	.	7. Load 8 MSB from bus 307
.	.	into RAM 350Y.
.	.	8. Load zeros into RAM 350Z.
.	.	9. Same as DE- CISION IIB (R = 1) 3.
6. DECISION VC.	2. DECISION VC.	10. DECISION VC.
DECISION VC:	Is word count in register 320 B = 0? YES—STEP IA	NO—DECISION VA
VI. LOAD A INSTRUCTION—LDA (4)		
STEP VIA:	Same as STEP IIA.	
DECISION VIA:	DAV?	NO—DECISION VIA
DECISION VIB:	What is R?	
	R = 1	R = 2
1. Load 16 LSB from bus 307	1. Same as DE- CISION VIB (R = 1) 1	1. Load 16 LSB from bus 307 into RAM 350X.
into RAM 350X.	.	2. Set DAR, wait for DAV.
2. Set DAR, wait for DAV.	through 6, ex- cept load 16	3. Load 8 MSB from bus 307
3. Load 16 LSB from bus 307	MSB at 1, 3, and 5.	into RAM 350X.
into RAM 350Y.	.	4. Set DAR, wait for DAV.
4. Set DAR, wait for DAV.	.	5. Load 16 LSB from bus 307
5. Load 16 LSB from bus 307	.	into RAM 350Y.
into RAM 350Z.	.	6. Set DAR, wait for DAV.
6. Same as DE- CISION IIB (R = 1) 3.	.	7. Load 8 MSB from bus 307
.	.	into RAM 350Y.
.	.	8. Set DAR, wait for DAV.
.	.	9. Load 16 LSB from bus 307
.	.	into RAM 350Z.
.	.	10. Set DAR, wait for DAV.
.	.	11. Load 8 MSB from bus 307
.	.	into RAM 350Z.
.	.	12. Same as DE- CISION IIB (R = 1) 3.
7. DECISION VIC.	2. DECISION VIC.	13. DECISION VIC.
DECISION VIC:	Is word count in register 320 B = 0? YES—STEP IA	NO—VIA
VII. RECALL X—RCX (5)		
STEP VIIA:	Clear address counter 320A (CLR).	
DECISION VIIA:	DAV?	NO—DECISION VIIA
DECISION VIIIB:	What is R?	
	R = 2 (16 bit)	R = 3 (24 bit)

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TRANSLATION STAGE 60—CONTROL LOGIC FLOW TABLE

1. Load 16 MSB from bus 307 into RAM 350X.	1. Load 16 LSB from bus 307 into RAM 350X.
2. Set DAR, wait for DAV.	2. Set DAR, wait for DAV.
3. STEP XIIA.	3. STEP XIIA.
4. Set DAR, wait for DAV.	4. Set DAR, wait for DAV.
5. STEP XIIA.	5. STEP XIIA.

VIII. RECALL Y—RCY (6)

STEP VIIIA: Clear address counter 320A (CLR).

DECISION VIIIA:

DAV?

YES—DECISION VIIIB

NO—DECISION VIIIA

DECISION VIIIB:

What is R?

R = 2 (16 bit)	R = 3 (24 bit)
1. Load 16 MSB from bus 307 into RAM 350Y.	1. Load 16 LSB from bus 307 into RAM 350Y.
2. Set DAR, wait for DAV.	2. Set DAR, wait for DAV.
3. Load 8 MSB from bus 307 into RAM 350Y.	3. Load 8 MSB from bus 307 into RAM 350Y.
4. Set DAR, wait for DAV.	4. Set DAR, wait for DAV.
5. STEP XIIA.	5. STEP XIIA.

IX. RECALL Z—RCZ (7)

STEP IXA: Clear address counter 320A (CLR).

DECISION IXA:

DAV?

YES—DECISION IXB

NO—DECISION IXA

DECISION IXB:

What is R?

R = 2 (16 bit)	R = 3 (24 bit)
1. Load 16 MSB from bus 307 into RAM 350Z.	1. Load 16 LSB from bus 307 into RAM 350Z.
2. Set DAR, wait for DAV.	2. Set DAR, wait for DAV.
3. Load 8 MSB from bus 307 into RAM 350Z.	3. Load 8 MSB from bus 307 into RAM 350Z.
4. Set DAR, wait for DAV.	4. Set DAR, wait for DAV.
5. STEP XIIA.	5. STEP XIIA.

X. RECALL XY—RXY (8)

STEP XA: Clear address counter 320A (CLR).

DECISION XA:

DAV?

YES—DECISION XB

NO—DECISION XA

DECISION XB:

What is R?

R = 2 (16 bit)	R = 3 (24 bit)
1. Load 16 MSB from bus 307 into RAM 350X.	1. Load 16 LSB from bus 307 into RAM 350X.
2. Set DAR, wait for DAV.	2. Set DAR, wait for DAV.
3. Load 16 MSB from bus 307 into RAM 350Y.	3. Load 8 MSB from bus 307 into RAM 350X.
4. Set DAR, wait for DAV.	4. Set DAR, wait for DAV.
5. Load 16 LSB from bus 307 into RAM 350Y.	5. Load 16 LSB from bus 307 into RAM 350Y.
6. Set DAR, wait for DAV.	6. Set DAR, wait for DAV.
7. Load 8 MSB from bus 307 into RAM 350Y.	7. Load 8 MSB from bus 307 into RAM 350Y.
8. Set DAR, wait for DAV.	8. Set DAR, wait for DAV.
9. STEP XIIA.	9. STEP XIIA.

XI. RECALL A—RCA (9)

STEP XIA: Clear address counter 320A (CLR).

DECISION XIA:

DAV?

YES—DECISION XIB

NO—DECISION XIA

DECISION XIB: What is R?

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TRANSLATION STAGE 60—CONTROL LOGIC FLOW TABLE

$R = 2$ (16 bit)	$R = 3$ (24 bit)
1. Load 16 MSB from bus 307 into RAM 350X.	1. Load 16 LSB from bus 307 into RAM 350X.
2. Set DAR, wait for DAV.	2. Set DAR, wait for DAV.
3. Load 16 MSB from bus 307 into RAM 350Y.	3. Load 8 MSB from bus 307 into RAM 350X.
4. Set DAR, wait for DAV.	4. Set DAR, wait for DAV.
5. Load 16 MSB from bus 307 into RAM 350Z.	5. Load 16 LSB from bus 307 into RAM 350Y.
6. Set DAR, wait for DAV.	6. Set DAR, wait for DAV.
.	7. Load 8 MBS from bus 307 into RAM 350Y.
.	8. Set DAR, wait for DAV.
.	9. Load 16 LSB from bus 307 into RAM 350Z.
.	10. Set DAR, wait for DAV.
.	11. Load 8 MSB from bus 307 into RAM 350Z.
.	12. Set DAR, wait for DAV.
7. STEP XIIA.	13. STEP XIIA.

XII. RECALL LOAD—RCL (10)

STEP XIIA: (1) Load accumulator 370 (X, Y, and Z) with "Vo" from RAM 350 (X, Y, and Z) at address A = 0.
 (2) Unit increment address counter 320A (INC).
 (3) Load accumulator 370 (X, Y, and Z) with "-Vp" from RAM 350 (X, Y, and Z) at address A = 1 to form $Vt = Vo - Vp$.
 (4) Unit decrement word counter 320B (DEC).

DECISION XIIA: Is the face part of a three dimensional object (is 3D flag set)?

YES—STEP XIIIB	NO—STEP XIIIE
(Three dimensional case)	(Two dimensional case)

STEP XIIIB: (1) Wait for DAV.
 (2) Load Three D register 341 (LOAD).
 (3) Set DAR, wait for DAV.
 (4) DECISION XIIIB.

DECISION XIIIB: Is word count ≥ 4 ? Vertex pointers are packed four to one sixteen bit word.

YES—STEP XIIC	NO—STEP XIID
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STEP XIIC: (1) Wait for DAV.
 (2) Load Three D register 342.
 (3) Set DAR, wait for DAV.
 (4) STEP XIID.

STEP XIID: (1) Load address counter 320A with first vertex pointer "A" from register 310A.
 (2) Load scaler 360 with "S" from register 310B.
 (3) Load accumulator 370 with the ΔV data from RAM 350 as accessed by the pointer from the Three D buffers.
 (4) Clear address counter 320A.
 (5) Wait for DAR-T from Normalizer 380.
 (6) Enable FIRST VERTEX flag in CIF register.
 (7) Load the buffer register in accumulator 370 with the contents of the accumulator (LOAD-B).
 (8) Clear "S" register in scaler 360.
 (9) Clear accumulator 370.
 (10) Unit decrement word counter 320B.
 (11) Load H and N address register 386 with "A" (LOAD).
 (12) Load accumulator 370 with Vo.
 (13) Unit increment address counter 320A.
 (14) Load accumulator 370.
 (15) Load address counter 320A with vertex address from Three D register 341 or 342.
 (16) Load scale register within scaler 360.

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TRANSLATION STAGE 60—CONTROL LOGIC FLOW TABLE

(17) Load accumulator 370.	
(18) Clear address counter 320A.	
(19) Wait for DAR-T.	
(20) Repeat items 7, 8, 9, and 10 of STEP XIID	
(21) Same as STEP XIID items 12-19.	
(22) Same as STEP XIID items 7-10.	
(23) Load last vertex flag into CIF registers when B = 0.	
(24) DECISION XIID.	
DECISION XIID:	Is word count B = 0?
	YES—STEP IA
	NO—DECISION XIIE (Visibility Test)
STEP XIIE:	(1) Same as STEP XIID items 1 and 2. (2) Wait for DAR-T. (3) Same as STEP XIID item 7. (4) Set first vertex flag. (5) Load accumulator 370. (6) Increment address counter 320A. (7) Decrement word counter 320B. (8) DECISION XIIC.
DECISION XIIC:	Is word count B = 0?
	YES—STEP IA
	NO—STEP XIIF
STEP XIIF:	(1) Wait for DAR-T. (2) Same as STEP XIIE items 4-7 except set last vertex flag when B = 0. (3) DECISION XIIC.
DECISION XIIE:	Is product of Visibility Test positive or negative?
	POSITIVE—STEP IA
	NEGATIVE—STEP XIIG
STEP XIIG:	(1) Same as STEP XIID items 20-23. (2) DECISION XIIF
DECISION XIIF:	Is word count B = 0?
	YES—STEP IA
	NO—STEP XIIG
XII. COLOR INTENSITY FLAG—CIF (11)	
In this instruction the CIF registers are loaded with CIF data from bus 307. Word counter 320B is decremented after each load until B = 0.	
XIV. STRING INSTRUCTION—STG (12)	
In this instruction the initial face of a string of faces is processed from RAM 350 through translation stage 60 into rotation stage 62 as a string of light points or four sided faces. The vertices of the four sided faces are retrieved from RAM 350 in CCW order as described in "XI. RE-CALL A—RCA (9)."	
XV. LOAD H—LDH (13) AND LOAD N—LDN (14)	
In this instruction data is loaded into H/N address register 3 from data bus 307, and then into H/N RAM 410 as described in Section VI. H/N Ram 410 receives the data during an idle portion of its cycle.	

CLIPPING STAGE 63

ROTATION STAGE 62

FIG. 8A shows the logic-diagram for the processing of translated point coordinates (V_t) from translation stage 62. Each new V_t is loaded into multiplexers 416X, Y, and Z (Step I). The object code in CIF register 460 which accompanies each new V_t is examined to determine if the new V_t is associated with a 3D face requiring visibility testing (Decision A). If so, the dot product of $V_t \cdot V_n$ (from N RAMs 410X, Y, and Z) is calculated (Step II). The sign bit of the dot product reveals whether the 3D face is visible or not (Decision B). The vertex of visible 3D faces (Decision B—yes) and the remaining non-3D face vertices (Decision A—no) are multiplied by the three x three H matrix in H RAMs 410X, Y, and Z to provide the rotated vector $V_c - Z_c$ first, Y_c second, and X_c last (Step III). Each coordinate is loaded into registers 450X, Y, and Z as they are calculated (Decision C and D, Steps IV, V, and VI).

50 FIGS. 8 B and C show the logic diagram for the control of clipping stage 63. The first point coordinates are loaded into multiplexers 520 (Step 2) and the out-code (OC) for each point is determined by window circuits 510. The object code in CIF register 590 is examined to determine whether the first coordinate is really a polygon vertex (or line end point) or merely a single light point (Decision A). In the case of vertices (and end points), the next vertex (or other end point) is loaded and outcode (OC) determined (Step 4). The OC's are examined to determine if the edge defined by the two vertices crosses the $Z=0$ plane (Decision C). If the edge crosses the $Z=0$ plane, then the intersection point is determined by a binary search (Step 5). If the edges do not cross the $Z=0$ plane, then the OC's of both points are examined to determine if they both are in front of pilot's eye 220 ($Z=0$ plane) or behind pilot's eye 220 and therefore definitely not visible (Decision D). The endpoints of edges which intersect the $Z=0$

plane or which are completely in front thereof, are examined via their OC for visibility (Decisions F, G, and H, and Step 8). If both endpoints are out of view (Case 3) the OC's are examined to determine if clipping is required (Decision I). If both endpoints are in view (Case 1) or otherwise do not require clipping, the next vertex coordinates are loaded. If only one vertex is in view (Case 2) or clipping is otherwise required (Case 3), the edge is processed through the appropriate series of binary search routines based on the OC's (Decision J). The binary search routines determine the interception points of the edge with the left, right, bottom or top boundaries of image plane 262. Each interception point becomes a new vertex of a new polygon formed by the visible portion of the original polygon face.

EDGE STAGE 65

FIG. 8D shows the logic diagram for the control of projection stage 64, processor 706X and Y, and slope divider 740. The clipped points from clipping stage 63 are loaded into registers 610 for projection division (Step 1). The quotients (projected points) are forwarded from registers 640 to edge stage 65, where it is examined for face data (Decision A). Non face data such as points and line segments are forwarded immediately to FIFO memory 910. Each face data point is examined for a first vertex (Decision B), which are loaded in V1 register 718 and current Yd multiplier register 710 (Step 2). Each non first vertex is loaded into register 710 as the current Yd and the previous Yd is advanced to register 716 (Step 3). Xd is similarly processed through processor 706X. Delta X and delta Y are calculated from their current and previous values, and loaded into registers 724 (Step 4). When the last vertex becomes the previous vertex in register 716 (Decision C), the face is closed by advancing V1 from register 718 to register 710 as the current vertex (Step 5). The last slope is calculated from the previous vertex (Vlast) and the current vertex (V1) and entered into register 724. The slopes are calculated by slope divider 740 as the delta X's and delta Y's are provided (Step 6).

TEXTURE STAGE 72

FIG. 8E shows the logic diagram for the control of Yds sorter 750. Input face edges are loaded into sorter 750 and examined for horizontal edges—delta Y=0 (Decision D). Horizontal edges are forwarded to FIFO memory 910 (Step 7). The non horizontal edges are examined for a first edge (Decision E). The first edge is entered at the start of the sort list (Step 8). Non first edges are examined to determine whether the input Yds is less than the last or output Yds in sorter 750 (Decision F). Smaller input Yds are entered at the start of the sort list (Step 9). Larger Yds are examined for a last edge (Decision G). Last edge is entered in last place of sort list (Step 10). The second edge is loaded (Step 11) and examined for input Yds less than the last Yds in sorter 750 (Decision H). Smaller Yds are inserted in the sort list (Step 12). Larger Yds are examined for last edge (Decision I). Last edges are entered into the sort list (Step 13). If the input edge is not the last edge, the next edge is loaded (Step 14). The input edge is again examined for a last edge (Decision J)—return to Decision D of flow chart for non last edge, and output sorter 750 to FIFO memory 910 for last edge.

DISPLAY GENERATOR 44

Texture Stage 72

Texture Stage 72, shown in FIG. 9, provides miniraster data for the set of horizontal scan lines forming each face. The miniscan lines progressively increase and/or decrease in response to the face edge list (Xds, Yds, Xslope, and Ydt for each edge) from face generation stage 65. The miniraster data for each miniscan line includes the Xd coordinate of the left hand end point (XdL), the width of the miniscan line (W), the Yd coordinate (Yd scan), Zc and CIF.

The edge list is loaded into memory 910 in ascending Yd order by face order once each frame, and extracted in the same order twice each frame—once for the field of even miniscan lines, and once for the field of odd miniscan lines. X coordinate generators 920L and 920R provide XdLc and XdRc respectively for each miniscan line by combining Xds with the Xslopes of the two opposed edges of the face which contain the end points of the scan line. XdLs is incremented by the left hand slope (XL slope) to form each XdL, and XdRs is incremented by the right hand slope (XR slope) to form each XdR. Only generator 920 is shown in detail. Slope multiplexer 928 divides the XL slope by two (select START) for the first scan line of the even field. During the remainder of the display cycle, the XL slope is passed through slope multiplexer 928 without division (select ACC) to accommodate the proper height spacing between adjacent miniscan lines in the same field. Adder 930 combines the X coordinate of the previous scan line (XdLp) with the current XL slope to provide the current X coordinate (XdLc). Output multiplexer register 940 provides either XdLs (select START) or XdLc (select ACC) to miniraster data register 950. Subtractor 952 provides the width W of each scan line by subtracting XdLc from XdRc (output of generator 920R). The Y coordinate of the miniscan lines (Yd scan) is similarly formed by incrementing Yds with Yslope from Yslope generator 960. At the end of each edge, Yd scan equals or exceeds the Ydt on the left edge (YdLt) or right edge (YdRt). The signals Yd scan \geq YdLt and Yd scan \geq YdRt indicate to control logic 70 that the next XL slope or XR slope is required in Xd generators 920.

DETAILED DESCRIPTION

FIFO memory 210 may be a 2048 words \times 100 bits memory (two hundred 82S11's) for sequentially outputting the complete edge list twice each cycle. Memory 210 interfaces with the remainder of miniraster calculator 72 through a 100 bit register (twenty five 74S175's).

XL slope register 924 may be a 20 bit storage register (five 74S175's) for holding each new Xslope as they are provided by memory 910.

XL slope multiplexer 928 may be a 20 bit 2:1 multiplexer (five 74S157's) with the START input right shifted to provide a division by two. The START and ACC select are provided by control logic 70.

XL Adder 930 may be a 20 bit adder (five 74283's) for incrementing each previous X left coordinate (XdLp) by the current XL slope.

Limit multiplexer 934 may be a 20 bit 4:1 multiplexer (ten 74S153's) for preventing underflow and overflow when an edge approaches the display boundary. The

four inputs are XdLc (twice), all ones (overflow), and all zeros (underflow). The two select inputs are the sign bits of XdLc and XL slope. Underflow occurs when both sign XdLc and sign XL slope are negative. Overflow occurs when sign XdLc is negative and sign XL slope is positive.

XdLs register 938 may be a 12 bit register (three 74S175's) for holding the X coordinate of the starting end point of the current edge (Xds) as it is provided by FIFO memory 910.

Output multiplexer register 940 may be a 20 bit 2:1 multiplexer register (five 25S09's) for accumulating XdLc and outputting either XdLs or XdLc. The output is returned to adder 930 and forwarded to miniraster data register 950.

Miniraster data register 950 may be a 76 bit register (nineteen 74S175's) for holding the miniraster data (XdLc 12 bits, W 12 bits, Yd scan 12 bits, CIF 24 bits, and Z 16 bits).

Subtractor 952 may be a 12 bit subtractor (three 74283's and two 74S04's) for providing the width of each miniscan line ($W = XdRc - XdLc$) to register 950.

Yslope generator 960 may be a 12 bit register (three 74S175's) hardwired to specify the maximum number of miniraster scan lines per frame. This number defines the scan density or Yslope.

Yslope multiplexer 964 may be a 12 bit multiplexer (two 74S175's) similar in function to Xslope multiplexer 928.

Y Adder 968 may be a 12 bit adder (three 74283's) for combining the 12 bits of Yslope with the 12 bits of Y coordinate of the previous scan line (Ydp) to form the Y coordinate of the current scan line (Yd scan).

Multiplexer register 970 may be a 12 bit multiplexer register (three 25S09's) similar in function to output multiplexer register 940.

Ydt register 974 may be a pair of 12 bit registers (six 74S175's) for holding the Yd coordinates of the left hand edge termination point (YdLt) and the right hand edge termination point (YdRt) which are periodically forwarded by FIFO memory 910.

Comparator 978 may be a pair of 12 bit comparators (six 74S85's) for comparing Yd scan with YdLt and YdRt to determine the end of each edge.

DEFLECTION CONTROL 74

Deflection stage 74 receives Yd scan accompanied by a series of XdLc's and W's for generating the sweep voltages which provide the series of horizontal scan lines outlining each polygon face. Yd scan identifies vertical position of the first vertex. XdL identifies the left hand start of each scan line thereafter. W determines the length of each scan line. Conventional integrator techniques may be employed to provide the appropriate X and Y ramp deflection voltages. The Y ramp changes at a uniform rate starting at Yd scan to move the CRT beam vertically across the face being displayed. The X ramps change at a much faster rate starting from an XdL to move the beam horizontally a distance indicated by the associated W. Suitable deflection techniques are disclosed in detail in U.S. Pat. No. 3,999,308 entitled "Real-Time Simulation of a Point System Having Textured Areas as Viewed by a Moving Observer" issued on Dec. 28, 1976 to Robert Louis Peters.

VIDEO CONTROL 76

Video control 76 receives color and intensity data from CIF 660 in projection stage 64 for each face being displayed to control the color and display brightness of the scan lines forming that face. If desired, the display intensity may be attenuated by Zc data for range simulation. Suitable video control techniques are also disclosed in detail in U.S. Pat. No. 3,999,308.

FULL RASTER EMBODIMENT

If desired, the edge list from register 760 may be displayed on a full raster in the conventional frame manner across the entire screen of display device 82. The vertices of all visible polygon faces (or visible portions thereof) for each frame are sorted by Yds to arrange the vertices in display order by raster. Next, the contents of each scan line are sorted by Xds to arrange the vertices in display order by raster. Next, the contents of each scanline are sorted by Xds to arrange the vertices in order of display within each scanline. The resulting Yds - Xds sorted edge list with accompanying slope and Yds data is processed through a conventional full raster display generator which provides the necessary vertical and horizontal sweep voltage waveforms.

EDGE SMOOTHING DEVICE 78

FIG. 10 shows edge smoothers 1010B, 1010G, and 1010R for the three primary colors blue, green, and red of display device 82. The color data is passed through D/As 1014 and combined with the color data by means of weighting register network 1018. The resulting intensity-color signals are applied to the corresponding edge smoother 1010B, 1010G, and 1010R. Red edge smoother 1010R is shown in detail and includes high gain, wide bandpass amplifier 1020 with negative feedback impedance 1024 connected between output junction 1026 and input junction 1028. Amplifier 1020 has a plurality of feedback paths (FB:O through FB:N) each having one of a corresponding feedback capacitor (C:O through C:N) and double-throw single-pull switching devices (SW:O through SW:N). Each feedback path, having one terminal (output terminal 1032) connected to amplifier output junction 1026 and having the other terminal (switched terminal 1034) connected to the associated switching device. The switching devices operate to connect switched capacitor terminal 1034 to either ground or to amplifier input 1028 depending on the content of input register 1040. Register 1040 has binary places BP:O through BP:N, one for controlling each switch SW:O through SW:N. The size of the feedback capacitors C:O through C:N form a power of two series, each capacitor having twice the value of the preceding capacitor starting with C:O=C and ending with C:N=2^NC. By connecting the switched terminal 1034 of selected capacitors to input junction 1028 and grounding switched terminal 1034 of the remaining capacitors, the total feedback capacitance C:t may have any one of 2^N separate integer multiple values between "C" and "2×2^NC." The number contained in the N binary places of input register 1040 define which of the 2^N feedback capacitance values for C:t is in effect.

The value of the total feedback capacitance C:t has an inverse proportionate affect on the bandpass of amplifier 1020. Capacitance C:t lowers the upperpass limit shunting high frequencies at output 1026 to input 1028 where they are suppressed to a negligible value due to the high gain and negative feedback relationship. As a

consequence, the response time of amplifier 1020 is decreased causing color and intensity changes in the video data to occur gradually over a small scan distance. Without edge smoothing, each variation in color and intensity along a scanline has a very high rate of change and occurs almost instantaneously on display 82 (see FIG. 12c) producing a discrete difference in the display at that point along the scanline. A series of these discrete differences are displayed across a group of continuous scanlines to generate the edge of a face. The offset between the discrete differences along adjacent scanlines caused by the slope of an edge produces the undesirable "staircase" effect. The selectable response time of edge smoother 78 causes each discrete difference in intensity and color to have a selectable slower rate of change (see FIG. 12d) which creates blending over a short time of the initial intensity level into the subsequent intensity level. The "staircase" is dispersed across the slight scanning distance required for the blending of the discrete intensity differences. The edge smoothing or blending period is directly determined by the RC time constant total feedback capacitance C:t and feedback register 1024.

FIG. 11 shows the "i-th" feedback path of an embodiment of edge smoothing circuit 1010. Switching device SW:i is formed by two FETs, input FET 1110 and grounding FET 1120, each having one element connected to switched terminal 1034 of capacitance C:i. A high voltage (FB Enable) from binary place BP:i of input register 1050 activates input FET 1110 causing feedback capacitor C:i to be one of the selected capacitors forming the total feedback capacitance C:t. A low voltage (GRD ENABLE) from BP:i deactivates grounding FET 1120 to remove the ground from switched terminal 1034 of C:i.

Preferably, amplifier 1020 is operated in the full pass-mode, and then reduced to lower pass frequencies. Each feedback capacitor is therefore normally grounded (non-selected) by residual zeroes in input register 1050, permitting the charge thereon to follow the output voltage at junction 1026. Input junction 1028 has a quiescent point at virtual ground due to the high gain characteristics of amplifier 1020 and negative feedback resistance 1024. The input voltage at junction 1028 is continuously driven down by the feedback voltage generated by the feedback current through feedback resistance 1024:

$$V_{\text{input}} = V_{fb} = IFb \times R \ 1024$$

This normally virtual ground condition of input junction 1028 and the actual ground at switched terminal 1034 of each capacitor permits the capacitors to be switched into the associated feedback path without a significant change in the charge status of the capacitor. The switched terminal of the capacitor is switched from an actual ground potential to a virtual ground quiescent point which minimizes the feedback capacitive transient current incident upon switching.

The fullpass mode (C:t=0) corresponds to the fastest risetime, having the greatest ratio of change. The rise-time is extended from the steepest rise to a slower rise in response to SLOPE data. As each new edge is encountered during each scan, a new set of feedback capacitors is selected in response to the slope of that edge. If desired, the actual ground may be removed from switched terminal 1034 just before connecting switched terminal 1034 to the virtual ground of amplifier input injunction 1028. That is, the deactivating GRD DISABLE voltage

to grounding FET 1120 may precede the activating FB ENABLE voltage to feedback FET 1110 (as shown in FIG. 12a and b). The switching sequence is biased towards a harmless momentary floating status on switched terminal 1034, in order to avoid the opposite situation where input 1034 is momentarily forced to actual ground instead of the virtual ground quiescent point. The charge on capacitance C:t does not change during the brief floating period because the switching of deactivation of grounding FET 1120 also provides isolation between the video output at junction 1026 and the switching transients generated within grounding FET 1120 due to the small interelement capacitance therein. Deactivation switching noise from grounding FET 1120 cannot pass through the not yet activated switching FET 1110 and cause undesirable transients in the video signal to CRT displays 82. Switching FET 1110 is activated after the deactivating switching transients from grounding FET 1120 have expired. Similar activation switching transients generated in switching FET 1110 are not isolated from VIDEO, but are neutralized by a corresponding inverted transient applied to input injunction 1028 through compensation capacitance 1140. Capacitor 1140 is charged simultaneously with switching FET 1110 by an inverted FB ENABLE signal from inverter 1144. The resulting compensation transient appears at input junction 1028 at the same time as the activation switching transient from FET 1110. Interference cancellation reduces the transient impact of switching FET 1110 to a subvisible level.

DETAILED DISCLOSURE

Intensity D/A 1014 may be a high spud, low glitch, digital to analog converter (DDC Model ADH 030-8) for converting intensity and color digital data into an analog signal. Emitter coupled logic compatibility is preferred for high speed applications.

Weighting resistors 1018 may be thermally stable, low capacitance, precision resistors for mixing the intensity data and color data. The resistive value may vary depending on the value of impedance 1024, the gain of amplifier 1020 and the desired weighting between intensity and color. For a 50/50 weighting at a gain of two, with an 800 ohm resistor 1024, the preferred value of each of the six weighting resistors 1018 is about 400 ohms.

Amplifier 1020 may be a high frequency, high slew rate operational amplifier (M. S. Kennedy model 750) with the non-inverting input connected to the reference potential-ground.

Impedance 1024 may be a resistor having a resistance of from about 500 to about 1000 ohms, 800 being preferred for the model 750 amplifier.

A thermally stably low capacitance precision resistor is preferred.

A stabilizing capacitor of about 10 p.f. may be connected across the resistor for minimizing overshoot and undershoot.

R-C network 1030 may be a 220 p.f. capacitor connected across an 82 ohm resistor, for minimizing undesirable operational amplifier transients which cause the feedback waveform to deviate from the ideal R-C response curve. Such transients are especially objectionable during the initial portion of the response curve.

Input register 1040 may be an N bit line receiver (10125's) for independently activating the N switches.

Rise time controller 1050 may be an N bit line driver (10132's) for storing SLOPE data between clock periods and advancing SLOPE data to input register 1040 in response to CLK from control logic 70.

Switches 1110 and 1120 may be high speed FETS 5 (Signetics Quad Switch 5000B).

Capacitors C:1 through C:N may be low leakage mica capacitors. The values of a series of five capacitors suitable for a pixel dimension of about 25 nanoseconds and a feedback resistance of 800 ohms are: 10

C:0=30 pfs

C:1=60 fps (62 fps may be employed)

C:2=120 fps

C:3=240 fps

C:4=480 fps (470 fps may be employed) 15

Inventor 1144 may be formed by one section of the line receiver of register 1040.

Variable capacitor 1140 may be an external capacitor (0.5-2.0 pfs) for adjusting the compensation wave shape. 20

CONCLUSION

The object of this invention has been accomplished by providing an analog circuit with a series of switchable, capacitance feedback paths which may be selected to vary the response time of the analog circuit. The leading and trailing edges of intensity-color video data along each scan line are integrated or extended over time, causing a graded change in intensity and color along each face edge. The feedback pair of alternately activated switches in each path are responsive to slope data for each edge for increasing the intensity-color transition time as the slope of that edge approaches zero - the horizontal. One switch of each pair is serially connected in each feedback path, and completes the loop as that feedback path is selected. The other switch of each pair grounds the feedback capacitance when that path is not selected. Switching transients from the grounding switch are isolated from the video data by activating the series switch last during selection and deactivating the series switch first during unselection. Transient charge current across the feedback capacitors is minimized by maintaining the switched side of the capacitor at ground potential through the grounding switch while unselected. During switching, the capacitor is disconnected from ground and connected to the vertical ground at the amplifier input through the series switch. The collective R-C time constant of the selected feedback paths varies at the slope of the current edge and is generally equal to the pixel time period. 45

It will be apparent to those skilled in the art, that various changes may be made in the apparatus and techniques described without departing from the scope of the invention. For example: The scan lines could be vertical, in which case the desired video risetime would be directly proportional to the slope of the edge. Further, substantial edge smoothing may be effected by blending only the intensity data and permitting the color data to maintain a step change. Accordingly, the scope of the invention should be determined only by the wording of the following claims and their legal equivalents. 55

We claim as our invention:

1. An image data system responsive to digital image data including position data which defines the position of the vertices of polygon faces forming the image, and visual data which defines the visual characteristics of 65

each face, for providing edge smoothed digital display data to a raster type display device, comprising:

image processor means for receiving the image position data and providing display coordinates for each vertex of each polygon face;

display generator responsive to the display coordinates for determining the leading and trailing intersections of each face with each scanline of the display raster, and responsive to the image visual data for providing a video signal to the display device along each scanline between the leading and trailing intersections of each face for generating the visual characteristics for that face on the display; and

edge smoothing means for decreasing the rate of change of the video signal in each scanline at the intersection of that scanline and at least one edge of each face, for causing a more gradual change of the visual characteristic prior to that intersection into the visual characteristic subsequent to that intersection by extending or contracting the intersection transient period.

2. The image data system of claim 1, wherein the controlled rate of change of the video signal at the scanline intersection is a function of the slope of that face edge. 25

3. The image data system of claim 1, wherein the display raster is formed by a plurality of spaced parallel scanlines extending along a first direction and spaced from one another along a second direction, and the rate of change of the video signal across that face edge - scanline intersection, varies as the ratio of the spacing distance along the second dimension between adjacent scanlines divided by the distance along the first direction between adjacent intersections of that face edge. 30

4. The image data system of claim 2, wherein the controlled rate of change of the video signal is directly proportional to the slope of that face edge, and

$$\text{slope} = \delta 1 / \delta 2;$$

where $\delta 1$ is the spacing between adjacent scanlines and $\delta 2$ is the changing position along the second direction of adjacent intersections along that face edge.

5. The image data system of claim 4, wherein the scanlines are horizontal and $\delta 1$ is a vertical increment and $\delta 2$ is a horizontal increment.

6. The image data system of claim 4, wherein the image processor means provides the $\delta 1$ increment and the $\delta 2$ increment between adjacent face edge - scanline intersections along each face edge.

7. The image data system of claim 6, wherein the image processor means further comprise a slope generating means which provides the slope of each face edge in response to $\delta 1$ and $\delta 2$ for controlling the rate of change of the video signal during the transient period associated with that edge - scanline intersection.

8. The image data system of claim 7, wherein the edge smoothing means includes an amplifier having an input means and an output means with a plurality of selectable feedback paths between the input means and the output means responsive to at least one face edge slope for controlling the rate of change of the video signal.

9. The image data system of claim 8, wherein each feedback path includes:

a capacitor means having an output terminal connected to the amplifier output side of that feedback path, and having a switched terminal connected to

the amplifier input side of that feedback path when that feedback path is selected; and a switching means connected to the switched terminal of the capacitor means and responsive to the at least one face edge slope for independently selecting at least one of the feedback paths by switching the switched terminal of the capacitance means to the amplifier input side of that feedback path when that feedback path is selected.

10. The image data system of claim 9, wherein the amplifier means is a high gain, high pass operational amplifier with the inverting input thereof forming the input means and the noninverting input thereof connected to a reference potential.

11. The image data system of claim 10, wherein the amplifier means further includes a feedback impedance connected between the output means and the input means for maintaining a quiescent voltage at the input means virtually at the reference potential.

12. The image data system of claim 11, wherein the feedback impedance is a resistance.

13. The image data system of claim 11, wherein the feedback impedance is a resistance and a capacitance connected in series.

14. The image data system of claim 10, wherein the switching means in each of the plurality of feedback paths switches the switched terminal of the associated capacitor means to the amplifier input means when that capacitor means is selected and to the reference potential when that capacitor means is not selected.

15. The image data system of claim 9, wherein the capacitance values of the capacitor means in the plurality of feedback paths forms a series of progressively increasing values permitting the total selected feedback capacitance to have a number of possible values from the value of the smallest capacitor means to the value of the sum of the capacitor means.

16. The image data system of claim 15, wherein the number of selected feedback capacitance values C:fb is:

$$\text{Number of } C_{fb} = 2^N$$

where N is the number of feedback paths.

17. The image data system of claim 16, wherein the capacitance value of each capacitor means in the series one through N is double the capacitance value of the preceding capacitor means in the series, so that the capacitance value (C) of each capacitor means is:

$$C(i) = (2^i)C$$

where i is an integer giving the position of the capacitor means in the series of one through N, and where C is the capacitance value of the first capacitor in the series.

18. The image data system of claim 17, wherein the slope is a binary number, each bit of which increases the value by a power of two, and each switching means is responsive to the bit having the power of two corresponding to the power of two capacitance value of the capacitor connected to that switch.

19. The image data system of claim 15, wherein the reference voltage is approximately ground potential.

20. The image data system of claim 15, wherein each switching means is a double throw-single pole switching device.

21. The image data system of claim 15, wherein the switching means in each of the plurality of feedback paths comprises:

a feedback switch for connecting the switched terminal of the associated capacitance means to the amplifier input means; and

a reference switch for connecting the switched terminal of the associated capacitance means to the reference potential.

22. The image data system of claim 21, wherein the switched terminals of currently unselected capacitors which are about to be selected are disconnected from the reference potential by means of the reference switch prior to being connected to the amplifier input means by means of the feedback switch for isolating the input means from switching transients generated within the reference switch.

23. The image data system of claim 22, wherein the edge smoothing means further comprises;

compensation means for providing a compensation signal to the input means simultaneously with and of the opposite polarity to each slope signal, which causes the feedback switches to connect the switched terminal of the selected capacitors to the input means.

24. The image data system of claim 23, wherein the compensation means includes an external capacitor for each feedback switch having a capacitance substantially identical to the internal capacitance of that feedback switch.

25. The image data system of claim 21, wherein the switched terminals of currently selected capacitors which are about to be unselected are disconnected from the amplifier input means by means of the feedback switch prior to being connected to the reference potential by means of the reference switch for isolating the input means from switching transients generated within the reference switch.

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